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CHIP PACKAGE INTERACTION (CPI) AND ITS IMPACT ON THE RELIABILITY OF FLIP-CHIP PACKAGES

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CHIP PACKAGE INTERACTION (CPI) AND ITS IMPACT ON THE RELIABILITY OF FLIP-CHIP PACKAGES

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Dedication

To my family, parents and friends

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CHIP PACKAGE INTERACTION (CPI) AND ITS IMPACT ON THE RELIABILITY OF FLIP-CHIP PACKAGES

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Chip-package interaction (CPI) has become a critical reliability issue for flip-chip packaging of Cu/low-k chip with organic substrate. The thermo-mechanical deformation and stress develop inside the package during assembly and subsequent reliability tests due to the mismatch of the coefficients of thermal expansion (CTEs) between the chip and the substrate. The thermal residual stress causes many mechanical reliability issues in the solder joints and the underfill layer between die and substrate, such as solder fatigue failure and underfill delamination. Moreover, the thermo-mechanical deformation of the package can be directly coupled into the Cu/low-k interconnect, inducing large local stresses to drive interfacial crack formation and propagation. The thermo-mechanical reliability risk is further aggravated with the implementation of ultra low-k dielectric for better electrical performance and the mandatory change from Pb-containing solders to Pb-free solders for environmental safety.

These CPI-induced reliability issues in flip-chip packaging of Cu/low-k chips are investigated in this dissertation at both chip level and package level using high-resolution Moiré interferometry and Finite Element Analysis (FEA). Firstly, the thermo-mechanical deformation in flip-chip packages is analyzed using high-resolution Moiré interferometry. The effect of underfill properties on package warpage is studied and followed by a strategy study of proper underfill selection to improve solder fatigue life time and reduce the risk of interfacial delamination in underfill and low-k interconnects under CPI.

The chip-package interaction is found to maximize at the die attach step during assembly and becomes most detrimental to low-k chip reliability because of the high thermal load generated by the solder reflow process before underfilling. A three-dimensional (3D) multilevel sub-modeling method combined with modified virtual crack closure (MVCC) technique is employed to investigate the CPI-induced interfacial delamination in Cu/low-k interconnects. It is first focused on the effects of dielectrics and solder materials on low-k interconnect reliability and then extended to the scaling effect where the reduction of the interconnect dimension is accompanied with an increased number of metal levels and the implementation of ultralow-k porous dielectrics. Recent studies on CPI-induced crack propagation in the low-k interconnect and the use of crack-stop structures to improve the chip reliability are also discussed.

Finally, 3D integration (3DI) with through silicon vias (TSV) has been proposed as the latest solution to increase the device density without down-scaling. The thermo-mechanical reliability issues facing 3DI are analyzed. Three failure modes are proposed and studied. Design optimization of 3D interconnects to reduce the thermal residual stress and the risks of fracture and delamination are discussed.

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Chapter 1: Introduction

1.1 Cu/low-k interconnect technology

The exponential growth in device density has yielded high-performance microprocessors containing 2 billion transistors [1]. The continuing improvement in device performance requires scaling in feature size including gate length, gate dielectric thickness, junction depth, and interconnect line width, etc. As the minimum device dimensions reduce, resistive-capacitive delay (RC delay), cross talk, and power dissipation of the interconnect structure have become the performance-limiting factors for device design and development. To address these problems, new materials, processes and designs have to be implemented into the interconnect and packaging structures.

The RC delay from interconnects can be mitigated by reducing the resistivity of metal lines. For this purpose, copper (Cu), which has a lower resistivity (~1.8 μΩ·cm) than aluminum-copper (AlCu) (~3.3 μΩ·cm), has been implemented since 1997 to reduce the RC delay in the interconnect wirings. The effective resistivity of Cu wire is about 45% lower compared with Al lines (Figure 1.1) [2].

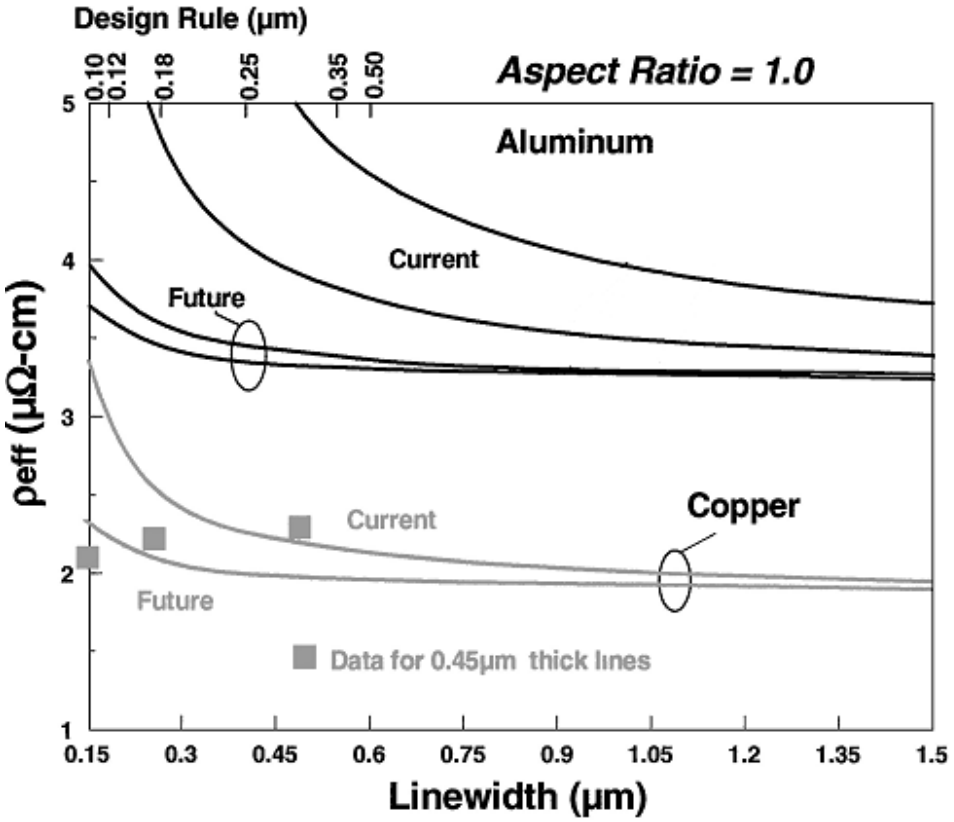


Figure 1.1: Resistivity change with decreasing metal line width for Cu and Al [2].

Cross talk, noise, power dissipation and distribution are additional performance issues caused by interconnect scaling, particularly for local and intermediate wiring levels. The capacitance increase induced by scaling raises the noise level and crosstalk between the metal lines and impacts the device performance. The capacitance of interconnect has two components: interline capacitance (C_{L-L}) and line-to-ground capacitance (C_{L-G}) as illustrated in Figure 1.2. With reduction of the feature size, the interline capacitance increases rapidly and eventually dominates the total capacitance for feature size below 1μm. (Figure 1.3) [3]. The interline capacitance is proportional to the dielectric constant of the inter-metal dielectric. Hence low-permittivity (k) dielectrics are

required to reduce the interline capacitance and also the total capacitance. Figure 1.4 illustrates the implementation of a low-k dielectric called carbon-doped oxide (CDO) by Intel Corp. in their Cu/low-k interconnect for 45nm technology [4].

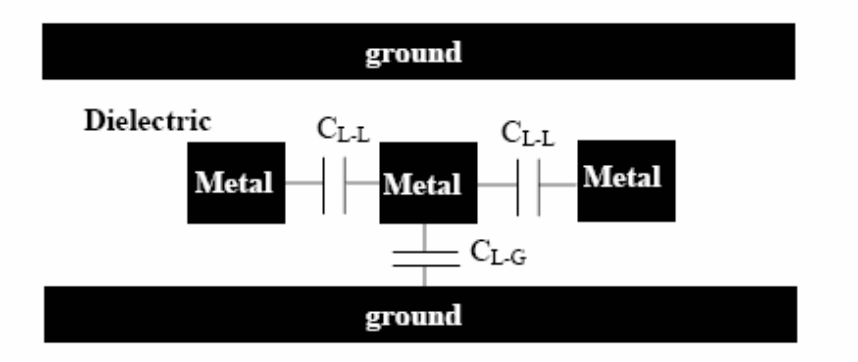


Figure 1.2: Diagram of interline capacitance, C_{L-L}, and line to ground capacitance, C_{L-G}. [3]

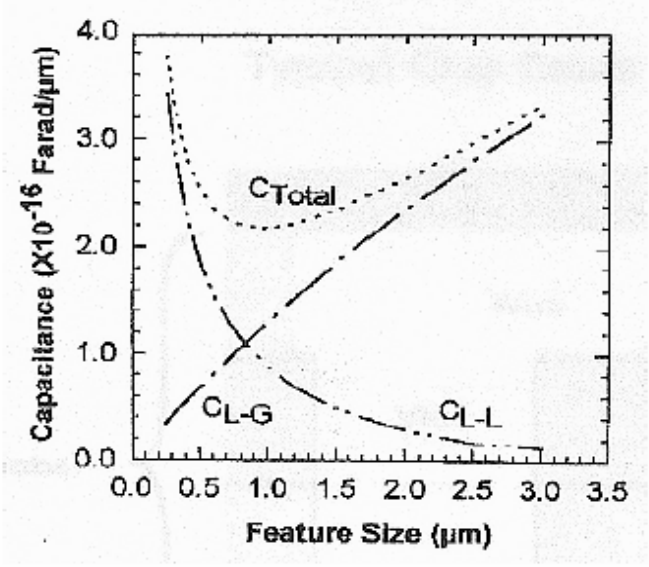


Figure 1.3: The line to ground, inter-line, and total capacitance vs. feature size [3]

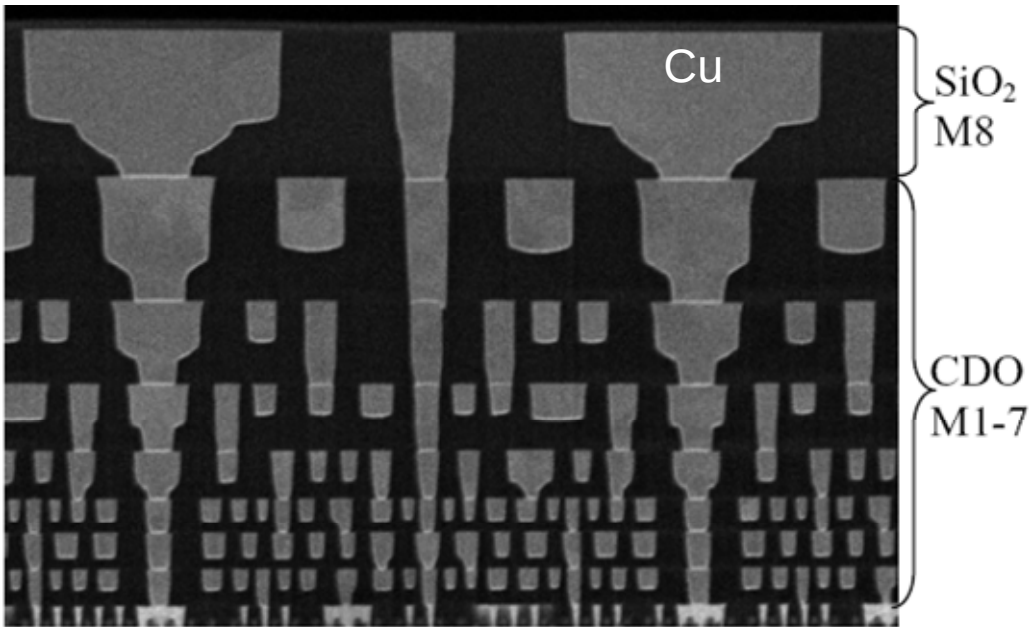


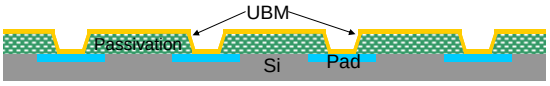
Figure 1.4: SEM image of Intel 45nm Cu/low-k interconnect structure [4]

1.2 Flip-Chip technology

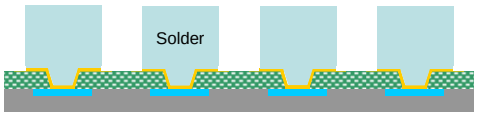
For advanced ICs, the packaging technology is mainly based on the flip-chip solder interconnects which is also called Controlled Collapse Chip Connection (C4) introduced by IBM in 1964. This type of first-level packaging structure provides interconnects between the active device side of the silicon die, face-down, and the multilayered wiring substrate through solder bumps. The area-array configuration has the capability to support the high input/output (I/O) pad counts and offer better electrical performance due to the increased device density and shorter interconnection length. The typical process sequence of flip-chip packaging is described in Figure 1.5. The first step is wafer bumping, in which the surface passivation layer on top of a completed wafer is patterned and the under bump metallization (UBM) layers are then electroplated into the pattern (Figure 1.5(a)). The UBM layers can provide good solder wetability, good

adhesion, and adequate electrical and mechanical connection between the device and the solders. After UBM electroplating, the portions of the UBM metal layers that are not needed are etched away. And solder alloy is then deposited on top of the patterned UBM layers as illustrated in Figure 1.5(b). When the solder deposition is done, the whole wafer is heated to reflow the bumps to form spherical solders (Figure 1.1(c)). Afterward, the wafer is diced into individual dies for subsequent packaging.

Before bonding to an organic substrate, the bumped die is flipped over and aligned with the substrate as shown in Figure 1.5(d). All the C4 solder connections are formed simultaneously by a solder reflow process (Figure 1.5(e)). The reflow temperature profile varies with solder materials. Finally a polymeric underfill is dispensed into the gap between die and substrate to reinforce the solder joints (Figure 1.5(f)).



(a)



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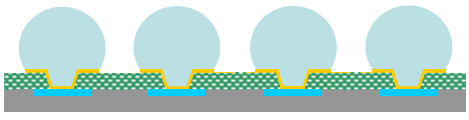

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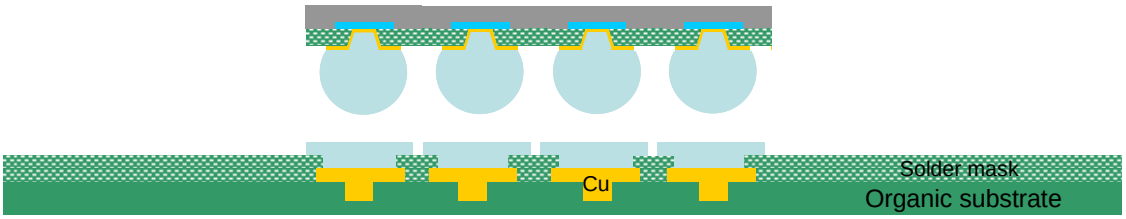
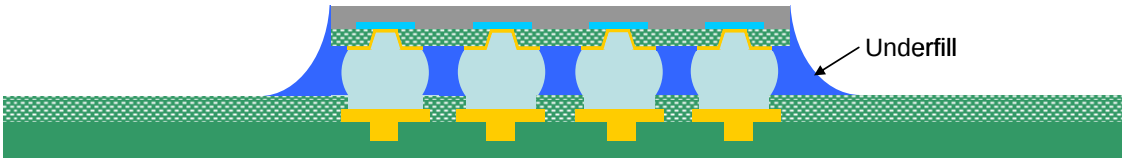


(d)

(e)



(f)

Figure 1.5: Assembly process flow for flip chip packages

With the implementation of Cu/low-k interconnects, the flip-chip package has also evolved. The advances include the emplyment of organic substrates with multilayered high-density wiring and solder bumps with pitch reducing from hundreds of microns to tens of microns. Although these developments contribute to the improvement in the electrical performance, they raise mechanical reliability concerns in solder joints and the Cu/low-k interconnects. The reliability issues in flip-chip packages are driven mainly by the mismatch in the coefficient of thermal expansion (CTE) between the Si die and the organic substrate [5, 6]. In addition, environmental safety has mandated the

switch from Pb-based solder materials to Pb-free solders which are more prone to thermal cyclic fatigue and electromigration failures [7, 8]. Besides the change in substrate and solder materials, implementation of ultra low-k dielectrics in Cu interconnect for improvement of electrical performance and the change of underfill materials to provide better protection for the solder bumps are two other main evolvements as shown in Figure 1.6. The structural reliability issues of low-k interconnect in flip-chip packages will be highlighted in the following section. And this is followed by two subsequent chapters describing the study of thermal deformation and stress characteristics and the underfill effect on reliability for flip-chip packages.

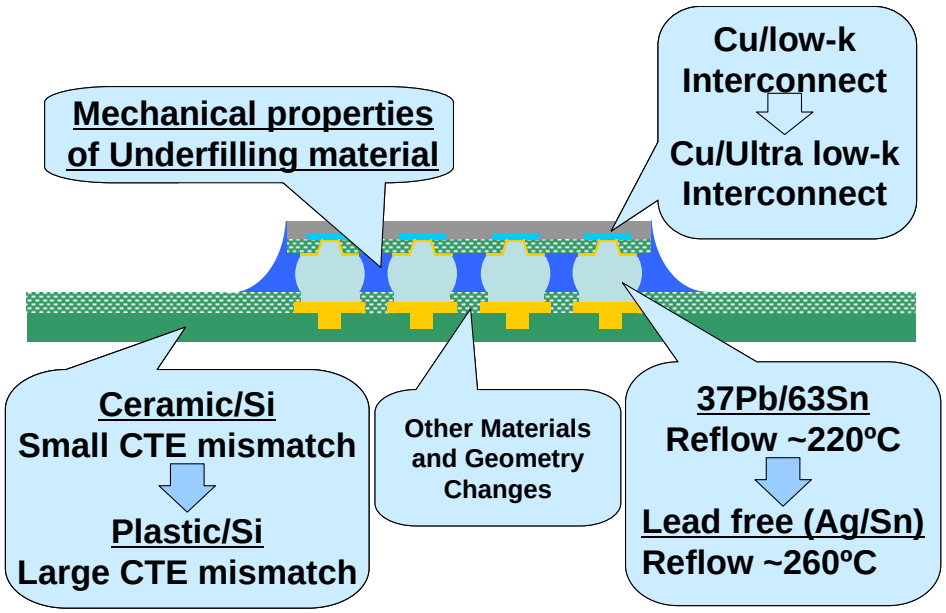


Figure 1.6: Major trends of flip chip packaging technology

1.3 Reliability issues of Cu/low-k interconnects in flip-chip packages

As the technology advances, the interconnect structure in the back end of the line (BEOL) continues to evolve with decreasing dimensions and increasing number of

layers and complexity. At this time, the effort of the semiconductor industry is focused on implementing ultralow-k (ULK) porous dielectric material ($k < 2.5$) into Cu interconnects to further reduce the RC delay [4]. However, mechanical properties of the dielectric materials deteriorate with increase in porosity, raising serious concerns on the integration of Cu/low-k interconnects. Wafer fabrication and subsequent packaging process are two major challenges for the Cu interconnect with low-k dielectrics. Two types of failure modes have been observed: cohesive fracture of the dielectrics [9-11] and interfacial delamination [12, 13]. The former pertains to the brittleness of low-k materials, and the latter manifests as a result of poor adhesion between the low-k and the surrounding materials.

During wafer fabrication, the interconnect structure is subjected to a series of thermal and mechanical processing steps such as film deposition, annealing and mechanical polishing. Low-k materials with poor mechanical properties are prone to fail during these processing steps. In addition, the interconnect structure as a whole is subjected to additional thermal stresses induced by the assembly processes, which may drive interfacial crack formation and propagation as shown in Figure 1.7.

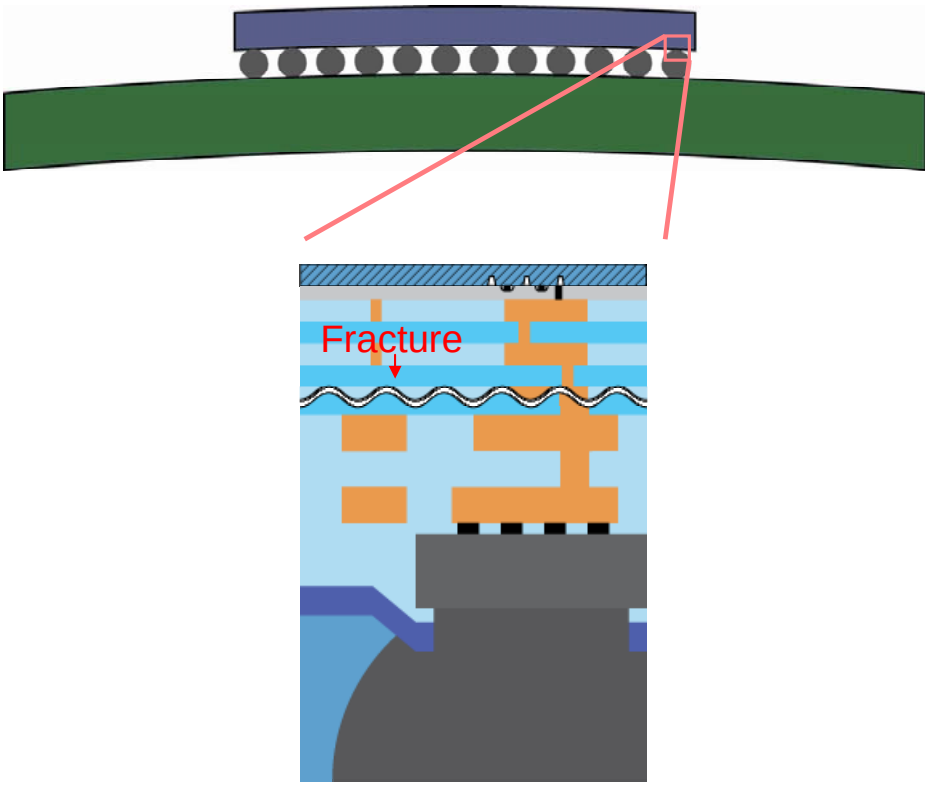


Figure 1.7: Fracture in a multilevel interconnect due to chip-package interaction (CPI)

Structural integrity is a major reliability concern for Cu/low-k chips during fabrication and when integrated into high-density flip-chip packages. The problem can be traced to the thermo-mechanical deformation and stresses generated by the mismatch in thermal expansion coefficients between the silicon die containing Cu/low-k interconnects and the package comprising the organic substrate [14]. Although the origin of the stresses in the in-chip interconnects and packaging structures is similar, the characteristics and the reliability impact for the low-k interconnects are distinctly different. At the chip level, the interconnect structure during fabrication is subjected to a series of thermal processing steps at each metal level including film deposition, patterning, and annealing. The nature of the problem depends, to a large degree, on the thermal and chemical treatments used in

the fabrication steps. For instance, for deposition of metal and barrier layers, the temperature can reach 400˚C and, for chemical-mechanical polishing (CMP), the chip is under mechanical stresses and exposed to chemical slurries simultaneously. When subjected to such process-induced stresses, the low-k interconnects with poor mechanical properties are prone to structural failure. Such mechanical reliability problems at the chip level have been extensively investigated [15].

When incorporated into the organic flip-chip package, the fabrication of the silicon die containing the interconnect structure has already been completed, so the interconnect structure as a whole is subjected to additional stresses induced by the packaging process. Here the maximum temperature is reached during solder reflow for die attach. The reflow peak temperature is about 220˚C or higher for eutectic Pb alloy solders and about 260˚C or higher for Sn-based Pb-free solders. During accelerated or cyclic thermal tests, the temperature varies from -55˚C to 150˚C or from 0˚C to 100˚C, depending on the protocol applied. Although the assembly or test temperatures for the package are considerably lower than the chip processing temperatures, the chip configuration in the flip-chip package is changed from the stand-alone configuration where very different stresses can exist in the low-k interconnect structure. The thermal stress in the flip-chip package arises from the mismatch of the CTE between the chip and the substrate; 2.6 ppm/°C for Si and about 17 ppm/°C for an organic substrate [6]. The thermally induced stress on the solder bumps reaches a maximum in the solder bumps located at the outermost row of the array, especially at the diagonal corners of the chip having the farthest distance from the neutral point (DNP). By using underfills, the stress at the solder bumps can be effectively reduced [16]. However, the underfill enhances the

package warpage by coupling the die and substrate, resulting in large stresses at the die-underfill interfaces [17, 18]. The thermo-mechanical deformation of the package can be directly transferred into the Cu/low-k interconnect structure in the BEOL, inducing large local stresses to drive interfacial crack formation and propagation. Such chip-package interaction and its reliability impact on Cu/low-k structures have received increased attentions recently [19-24].

1.4 Objective and Outline

The objective of this dissertation is to investigate the basic mechanisms of CPI-induced thermo-mechanical reliability issues in flip-chip packages, at both chip level and package level, and find proper ways to optimize the structure and material design to retain the package integrity. Both experimental techniques and finite element analysis (FEA) are used in the dissertation to analyze the reliability problems caused by CPI. In Chapter 2 the packaging-induced thermal deformation and stresses in flip-chip packages are analyzed using high-resolution moiré interferometry. Two kinds of packages, one with a heat spreader on top of the die and one without, are tested and compared. The moiré technique is also applied to study the effect of underfill properties on package warpage as described in Chapter 3. This is followed by a strategy study of proper underfill selection to improve solder fatigue life time and reduce the risks of interfacial delamination in underfill and low-k interconnect structures under CPI.

The chip-package interaction is found to be maximized at the die attach step during assembly and becomes most detrimental to low-k chip reliability because of the high thermal load generated by the solder reflow process before underfilling. A three-dimensional (3D) multilevel sub-modeling method combined with modified virtual crack

closure (MVCC) technique is introduced in Chapter 4 to investigate the CPI-induced interfacial delamination in Cu/low-k interconnects. The discussion is first focused on the effects of dielectric and solder materials on low-k interconnect reliability. Packaging-induced crack driving forces in ultra low-k layers are deduced and compared with those for fully dense low-k dielectrics. Methods to improve the mechanical reliability of Cu/low-k interconnect under CPI are presented. The discussion is then extended to study the scaling effect where the reduction of the interconnect dimension is accompanied by the use of more metal levels and the implementation of ultralow-k, porous materials. Recent studies on CPI-induced crack propagation in the low-k interconnects and the use of crack-stop structures to improve the chip reliability are discussed.

3D integration (3DI) with through silicon vias (TSV) has been proposed as the latest solution to increase the device density without down-scaling. Chapter 5 investigates the thermo-mechanical reliability issues of 3DI. Three failure modes are proposed and studied. Design optimization of 3D interconnects to reduce the thermal residual stress and the risks of fracture and delamination were discussed.

And finally, the summary of this dissertation and proposed future work are presented in chapter 6.

Chapter 2: Characterization of Thermo-Mechanical Behavior of Microelectronic Packages

2.1. Introduction

The large CTE mismatch between the die and substrate can cause the package to bend and generate significant thermal stresses in solder joints under thermal loads. Such stresses are harmful not only to the reliability of solder bumps but also to the stability of Cu/low-k interconnect especially at the proximity of solder UBM, raising mechanical reliability concerns in flip-chip packages. Characterization of the thermal deformation of flip-chip packages is therefore important for understanding the thermo-mechanical reliability issues. In this study, high resolution moiré interferometry is used to measure the deformation of flip-chip packages under pre-set thermal loadings.

Moiré interferometry is a whole-field optical interference technique with high resolution and high sensitivity for measuring the in-plane displacement and strain distributions [1]. The optical system of the interferometer is schematically shown in Figure 2.1 [2]. The incoming laser beam from the optical fiber is reflected by mirror 1 and 2 and then impinging onto the surface of the reference grating, which splits the laser beam into four beams (2U and 2V beams). The four laser beams are reflected onto the surface of the sample grating. A moiré image is formed by the interaction of the virtual grating created by the reference grating with the deformed specimen grating and recorded by the digital camera [2]. The displacement field and strain distribution can be deduced from the moiré images.

$$u = \frac{N_x}{f_s}, \quad v = \frac{N_y}{f_s} \tag{2.1}$$

$$\begin{aligned} \varepsilon_x &= \frac{\partial u}{\partial x} = \frac{1}{2 f_s}\frac{\partial N_x}{\partial x} \approx \frac{1}{2 f_s}\frac{\Delta N_x}{\Delta x} \\ \varepsilon_y &= \frac{\partial v}{\partial y} = \frac{1}{2 f_s}\frac{\partial N_y}{\partial y} \approx \frac{1}{2 f_s}\frac{\Delta N_y}{\Delta y} \\ \varepsilon_{xy} &= \frac{1}{2}\left(\frac{\partial u}{\partial x} + \frac{\partial v}{\partial y}\right) \approx \frac{1}{4 f_s}\left(\frac{\Delta N_y}{\Delta x} + \frac{\Delta N_x}{\Delta y}\right) \end{aligned} \tag{2.2}$$

where u is the displacement along the x direction, v is the displacement along the y direction. N_x, N_y are the fringe order of the u, v field moiré fringe pattern respectively and f_s is the frequency of the specimen grating.

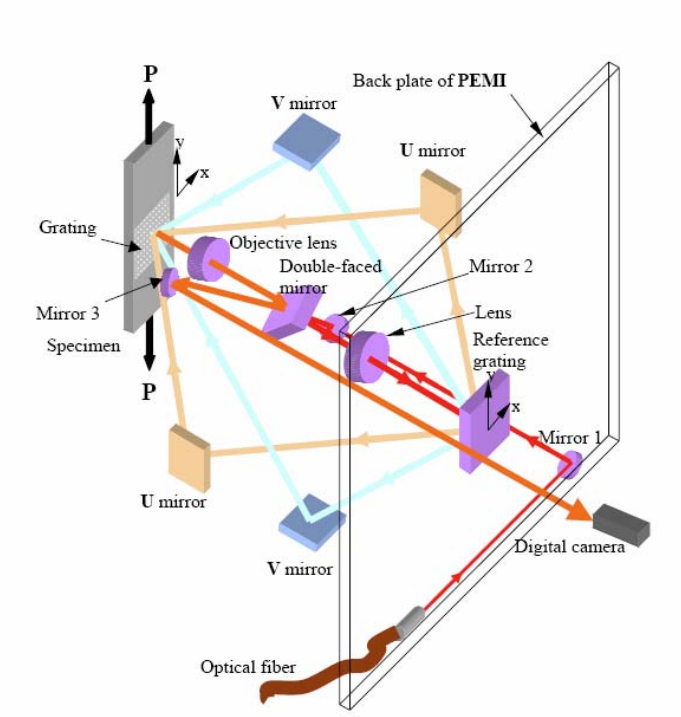
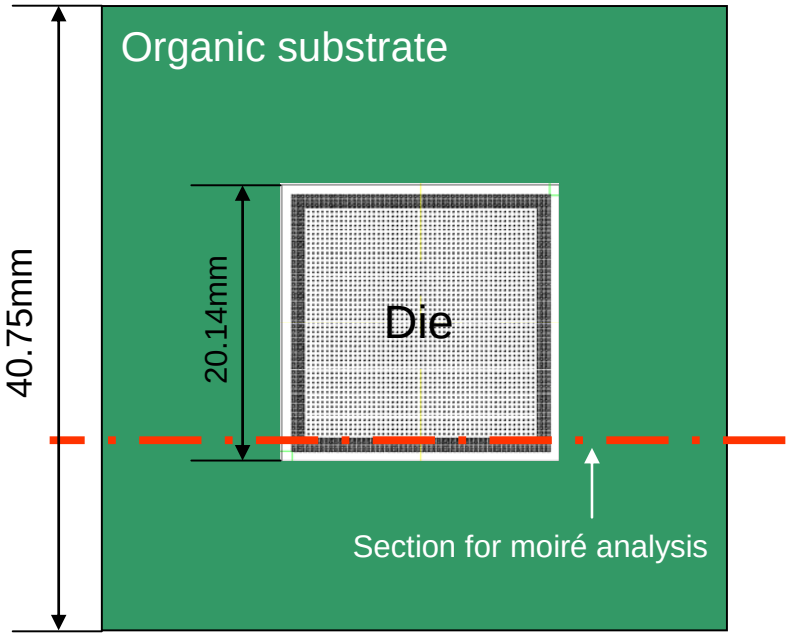


Figure 2.1: Optical system of moiré interferometer (taken from [2])

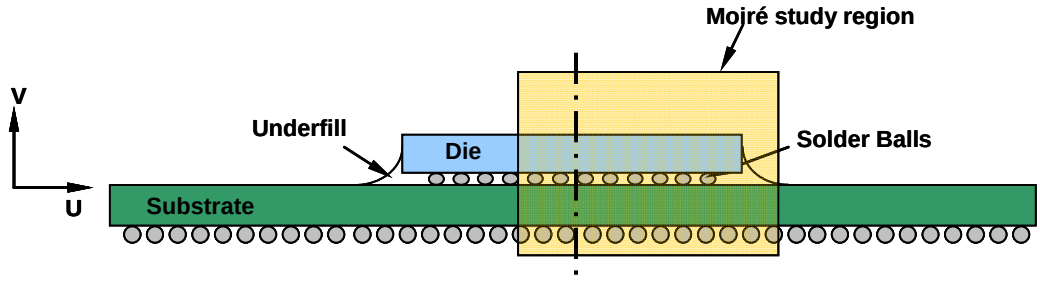
This method has been successfully used to measure the thermal-mechanical deformation in electronic packages to investigate package reliability [2-6]. A sensitivity of 417nm per fringe contour can be reached with a specimen grating of 1200 lines/mm.

2.2 Sample preparation and measurement

Two types of packages were analyzed in this study. Both of them were built with 47.5mmx47.5mm organic substrates and 20mmx20mm Si dies as shown schematically in Figures 2.2(a) (lidless) and 2.3(a) (with lid). These two packages were identical except that the latter had a lid on top of the package as a heat spreader while the former did not. The red dash line in the diagrams indicates the cross-section analyzed in the test, which is the first row of the solder bump array along the polishing direction. Each specimen was cut at the die edge first and then polished inward to expose the cross-section of interest. The detailed sample preparation process can be found in reference 2. Figures 2.2(b) and 2.3(b) illustrate the cross section views of these two packages, respectively. The yellow blocks denote the areas analyzed during the moiré test.

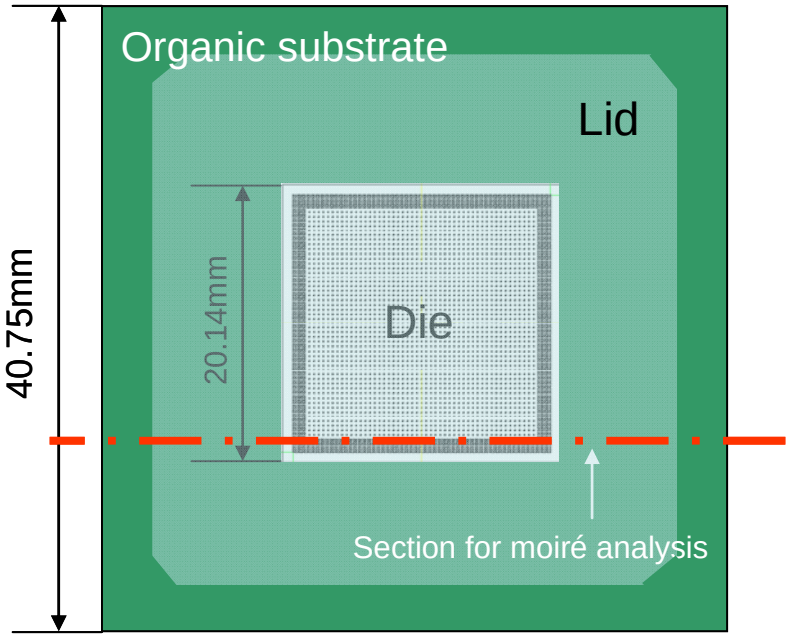


(a)

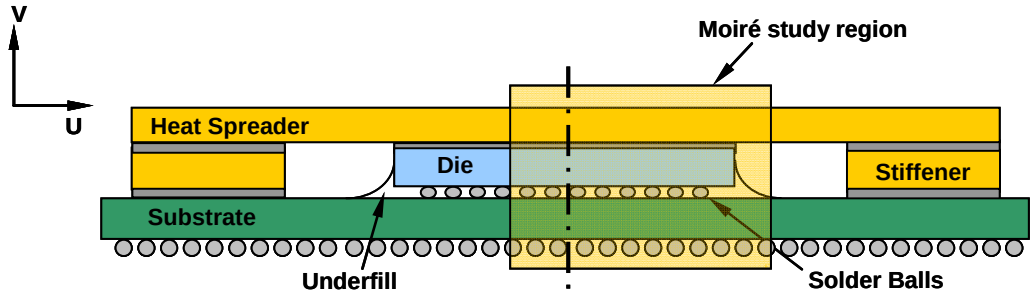


(b)

Figure 2.2: Schematics of flip-chip packages without lid (a) top view (b) cross-sectional view along the red line



(a)



(b)

Figure 2.3: Schematics of flip-chip packages with lid as a heat spreader (a) top view (b) cross-sectional view along the red line

After treating the polished surface with acetone, a low-viscosity, brittle adhesive was used to adhere a 1200 lines/mm grating on the polished surface of the specimen at a temperature of 82^{o}C. The deformation at this temperature was taken as that of a reference state. The moiré test was performed at the room temperature, 22^{o}C, providing a thermal loading of -60^{o}C. The thermal load that can be used for moiré studies is limited by the

glass transition temperature (Tg) of the underfill. An optical microscope picture of the cross-section is shown in Figure 2.4. Only the region close to die edge that usually has the largest thermal strain in the package was analyzed in the moiré test.

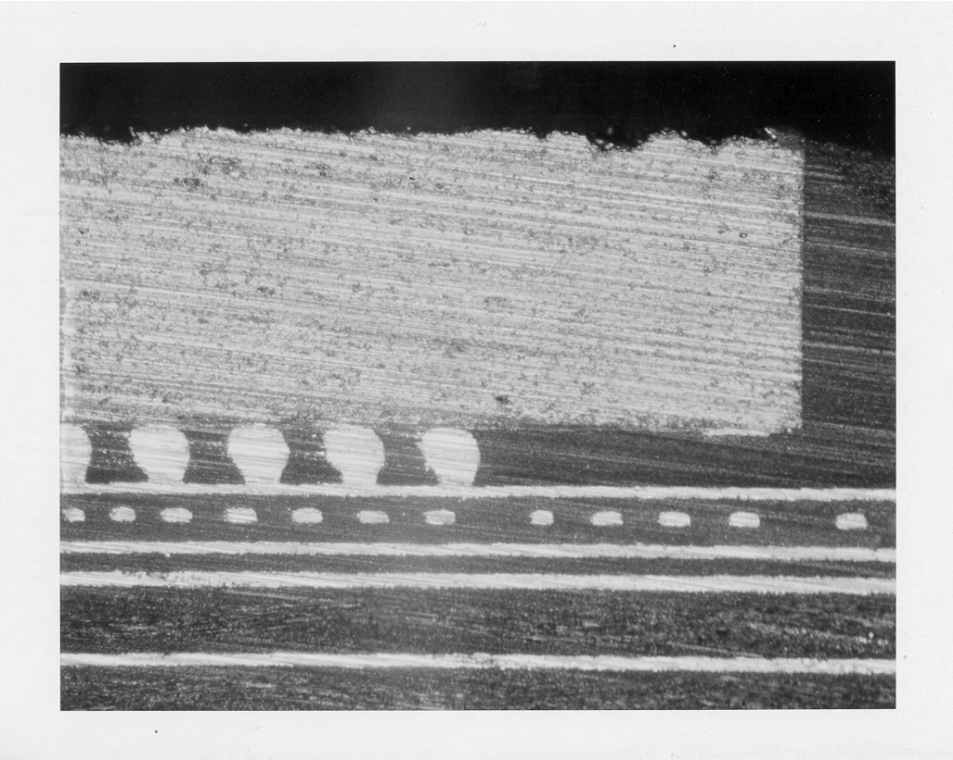


Figure 2.4: Optical picture of sample cross-section

The equipment used in the moiré test is a modified IBM Portable Engineering Moiré Interferometer (PEMI) system as shown in Figure 2.5 [2]. The high-resolution moiré interferometry is a very sensitive measurement technique and careful system alignment is required before each measurement in order to obtain quality images for high accuracy. A standard 1200 lines/mm grating was first put on the sample holder to align the optical system as a reference grating. After the system was carefully aligned, the prepared sample was evaluated by following the steps outlined in reference [2]. The moiré fringe patterns were then recorded and analyzed.

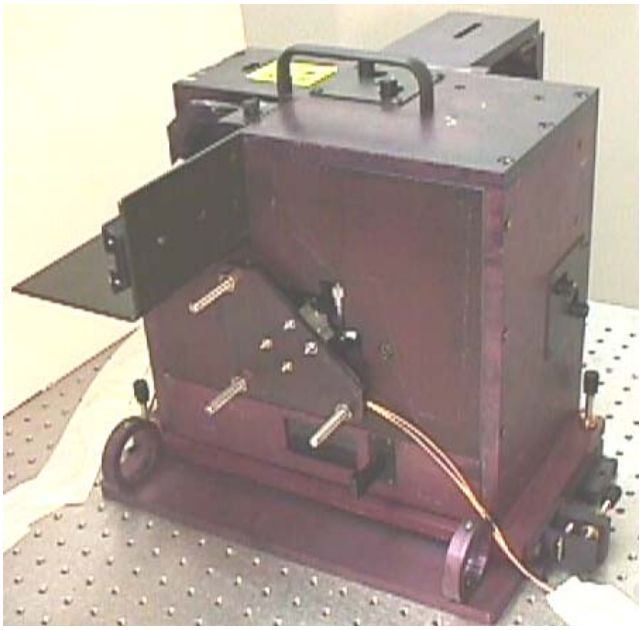


Figure 2.5: Modified PEMI for moiré test (take from [2])

2.3 Results and discussion

The package without lid (Figure 2.2) was first tested. The fringe patterns obtained under a thermal load of -60^{o}C are shown in Figures 2.6(a) and 2.6(b). The U and V fields in the diagram denote the deformation pattern along the vertical and horizontal directions, respectively. Each fringe represents a displacement of 417nm in this case. Package bending can be deduced from the V field pattern by counting the number of fringes in the image.

The precision of the regular moiré tests is limited by the ability to interpolate the moiré fringes, which is rather restricted since the fringe pattern appears as a series of broad dark lines. This is evidenced by the fact that the fringe pattern in the solder layer can not be resolved in the regular U and V moiré images shown in Figures 2.6(a) and

2.6(b). The standoff height of solder joints in the package between the die and the substrate is less than 100μm which is too small to reveal any details by the whole field image. Therefore, a high resolution moiré test based on phase shifting technique was employed to investigate the deformation near the solder layer which will be discussed later in this chapter.

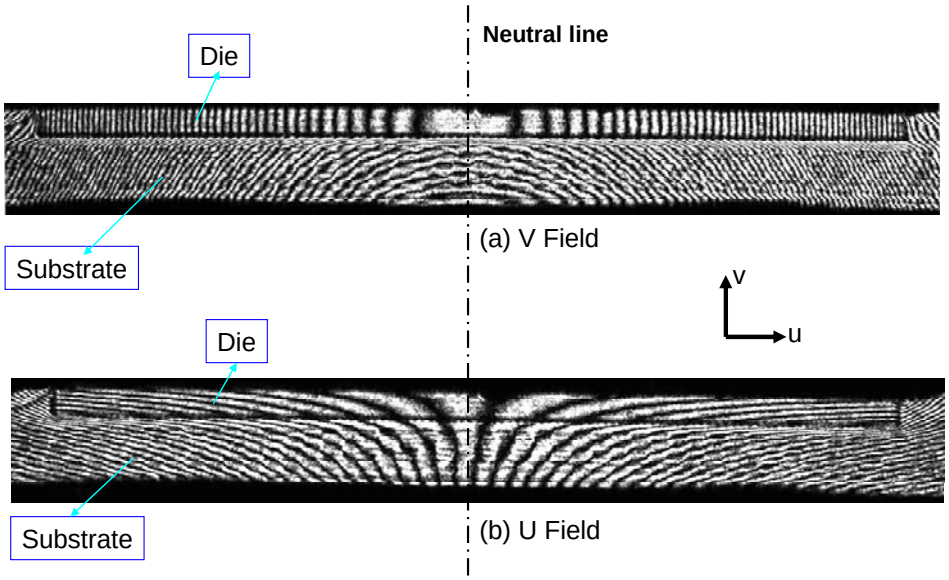
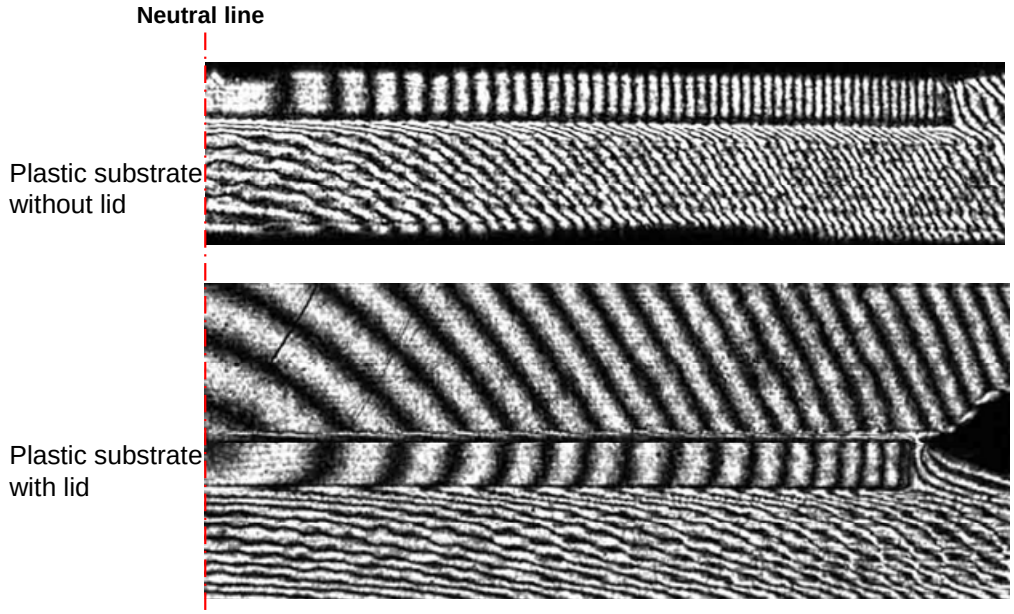
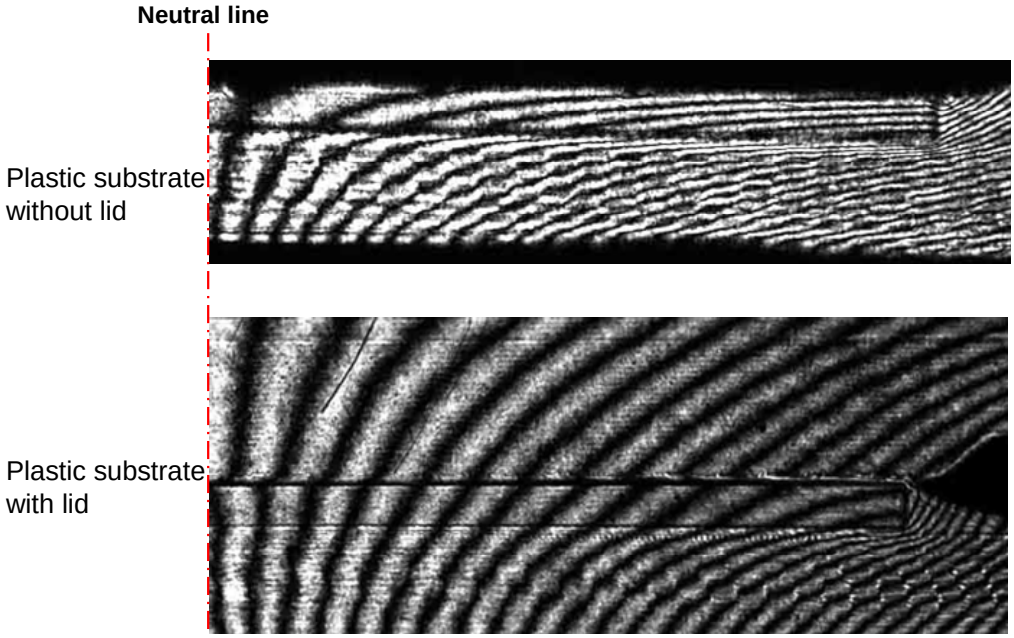


Figure 2.6 Fringe patterns for package without lid for a thermal loading of -60°C (a) V field (b) U field

The package with lid on top was also tested under the same thermal load, and a comparison of the fringe patterns between these two packages are given in Figure 2.7. The most important observation is that the number of fringes in the die for package with lid is far fewer than that of the lidless package, indicating a smaller die bending. The results obtained from moiré analysis are shown in Figure 2.8 where a reduction of 75% in die bending was found by applying a lid on top of package to restrain the package warpage.



(a) V field



(b)

Figure 2.7: Comparison of regular moiré image pattern between packages with lid and without lid (a) V field (b) U field

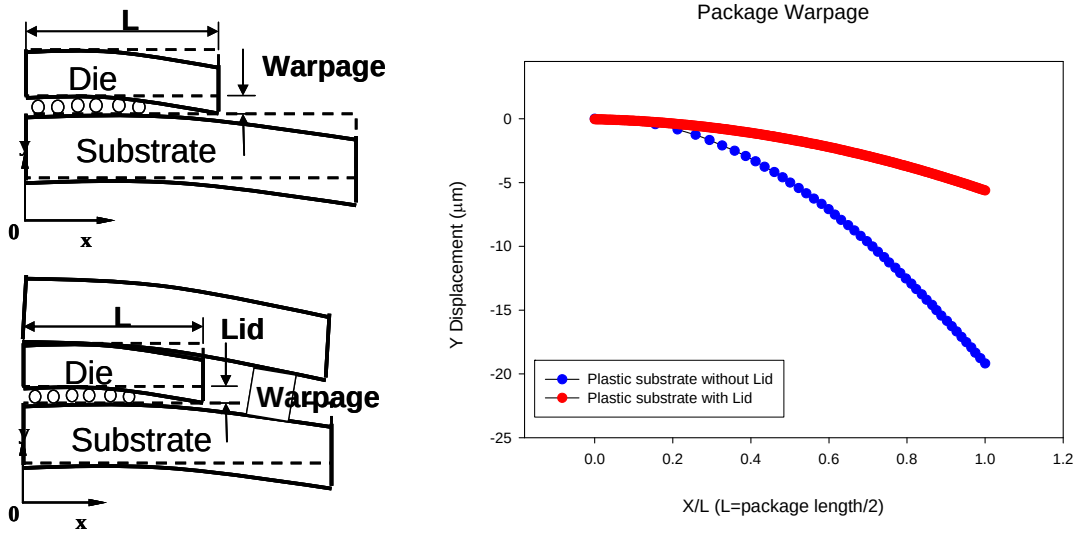


Figure 2.8: Comparison of warpage in the die for package with and without lid

For both packages, a mismatch in the fringes at the die/lid interface can readily be observed in both V and U images. This can be attributed to the CTE mismatch across this interface. Figure 2.7 shows that the die corner was the critical area because the displacement gradient between die and substrate reached its maximum value at this location, and, therefore, the highest strain was developed. This is to be expected since the mismatch in thermal and mechanical properties between the die and the lid produces singular stresses at the bimaterial apex at the interface [7, 8].

The sensitivity of 'regular' Moiré interferometry should be adequate for assessing the overall thermal deformation, but it is not sufficient for measuring thermal deformation in high-density electronic packages, particularly for small features, such as solder balls. Therefore a high resolution moiré measurement of these packages is required with improved resolution at local areas such as the die corner. In a regular moiré pattern, the spacing between fringes corresponds to a phase angle difference of 2π, which is

417nm in displacement. Between two interference fringes, the phase angle varies continuously, which cannot be determined explicitly from the regular moiré pattern. However, the change of the phase angle can be captured by the phase-shifting technique in which four continuous images are taken with a phase different of π/2 and then combined as in Eq. 2.3 and Eq. 2.4 to extract the phase angle between fringes.

$$\begin{aligned} I_1(x,y) &= I_0(x,y) + I'(x,y)\cos[\phi(x,y)] \\ I_2(x,y) &= I_0(x,y) + I'(x,y)\cos[\phi(x,y)+\pi/2] \\ &= I_0(x,y) - I'\sin[\phi(x,y)] \\ I_3(x,y) &= I_0(x,y) + I'(x,y)\cos[\phi(x,y)+\pi] \\ &= I_0(x,y) - I'\cos[\phi(x,y)] \\ I_4(x,y) &= I_0(x,y) + I'(x,y)\cos[\phi(x,y)+3\pi/2] \\ &= I_0(x,y) + I'\sin[\phi(x,y)] \end{aligned} \qquad (2.3)$$

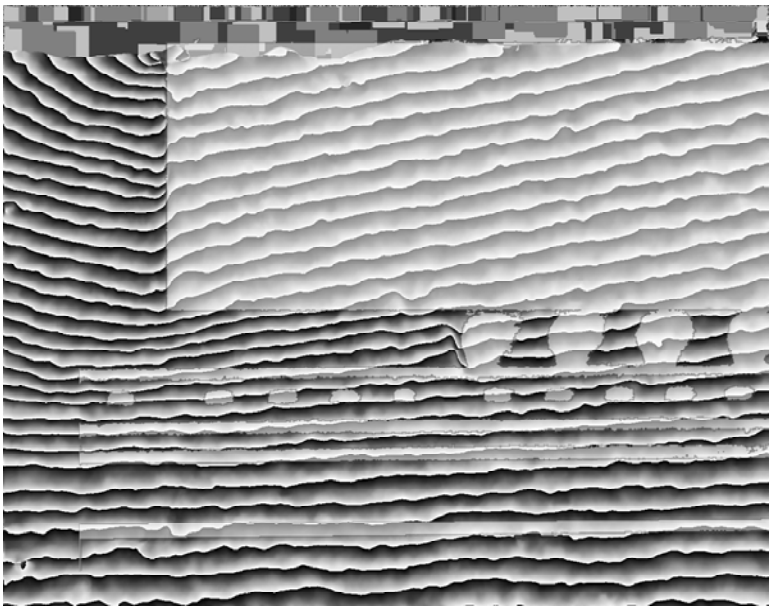
where $I_o(x,y)$ and $I'(x,y)$ are the background and periodically varying intensities in the interference pattern and $\phi(x,y)$ is the phase angle of the interference pattern at each pixel location (x,y). The phase angle is then determined as

$$\phi(x,y) = \arctan\left[\frac{I_4(x,y) - I_2(x,y)}{I_1(x,y) - I_3(x,y)}\right] \qquad (2.4)$$

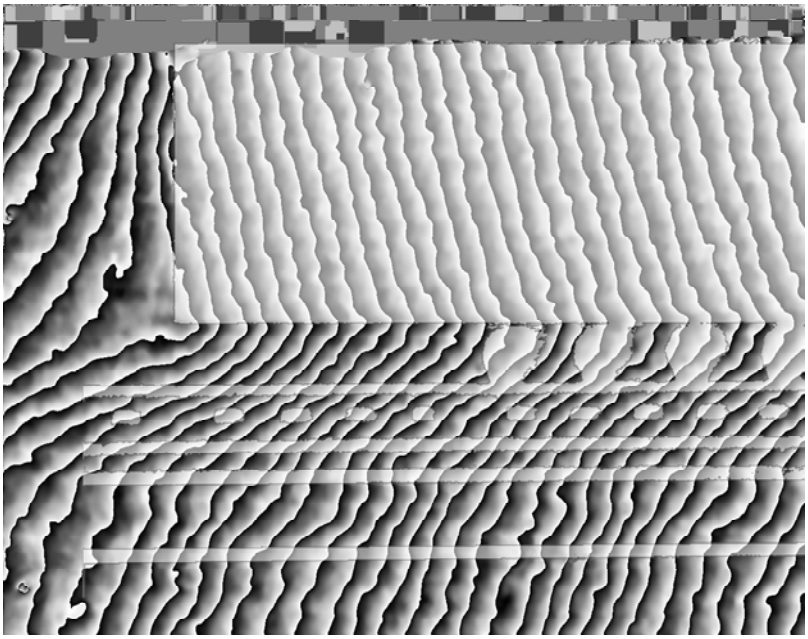
Once the phase angle distribution between two interference fringes is obtained, the displacement distribution can be determined by measuring the change of the phase angle (Eq. 2.5).

$$\begin{aligned} u(x,y) &= \frac{1}{2f_s}\frac{\phi_u(x,y)}{2\pi} \\ v(x,y) &= \frac{1}{2f_s}\frac{\phi_v(x,y)}{2\pi} \end{aligned} \qquad (2.5)$$

A high resolution phase shifted moiré analysis was carried out at the die corner for both packages. The phase maps obtained are shown in Figures 2.9 and 2.10. Optical images of the cross-section were superimposed onto the phase maps to identify the locations of the deformation. The die edge can be clearly identified from the high displacement gradients at the interface where a large strain was clearly observed. In these phase maps, each contour corresponds to 208nm displacement. The phase map can be subdivided to obtain displacement contours with resolution reaching 26 nm as shown in Figure 2.11 and 2.12.

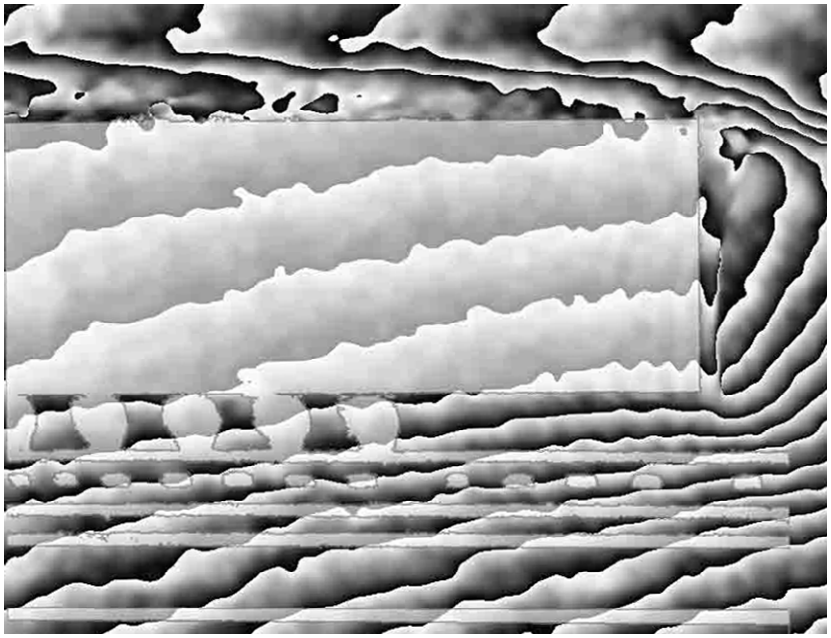


(a) U Field

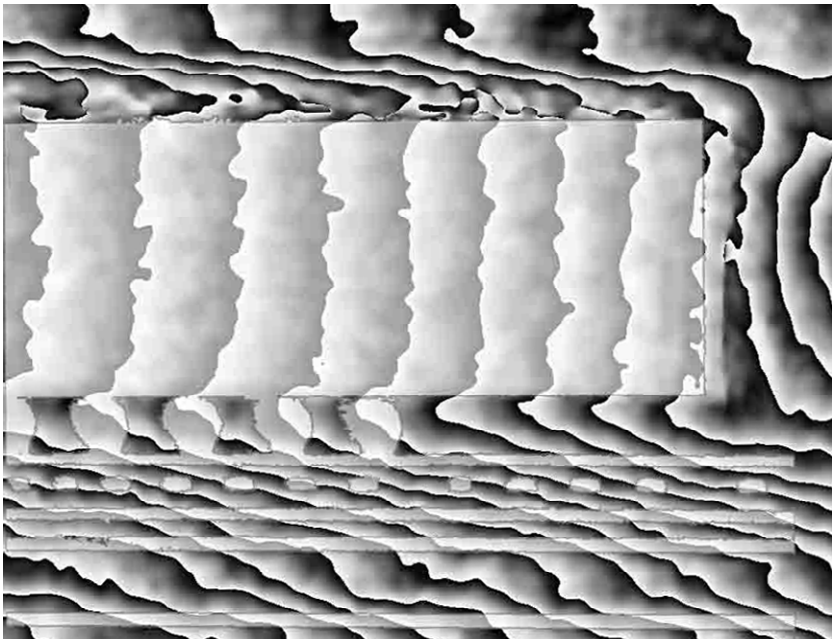


(b) V Field

Figure 2.9: Phase maps for package without lid (a) U filed (b) V field

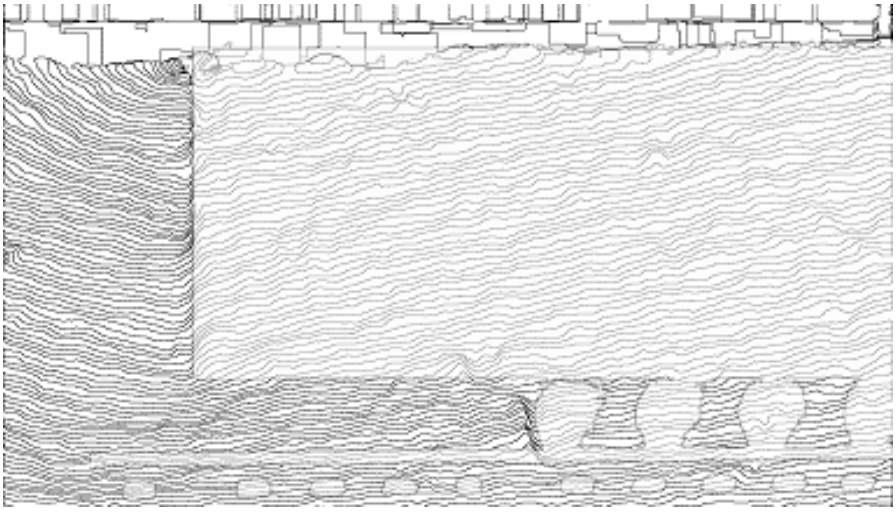


(a) U Field

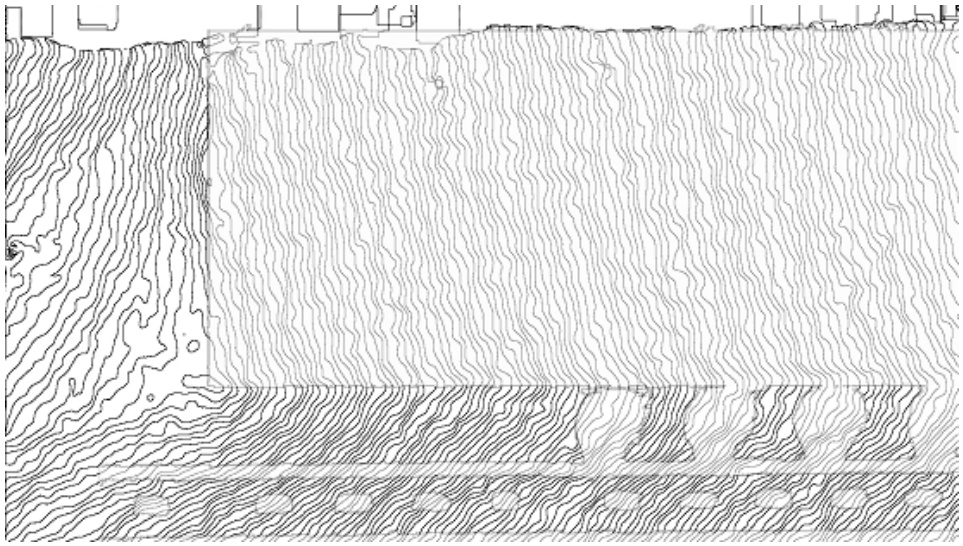


(b) V Field

Figure 2.10: Phase maps for package with lid (a) U filed (b) V field

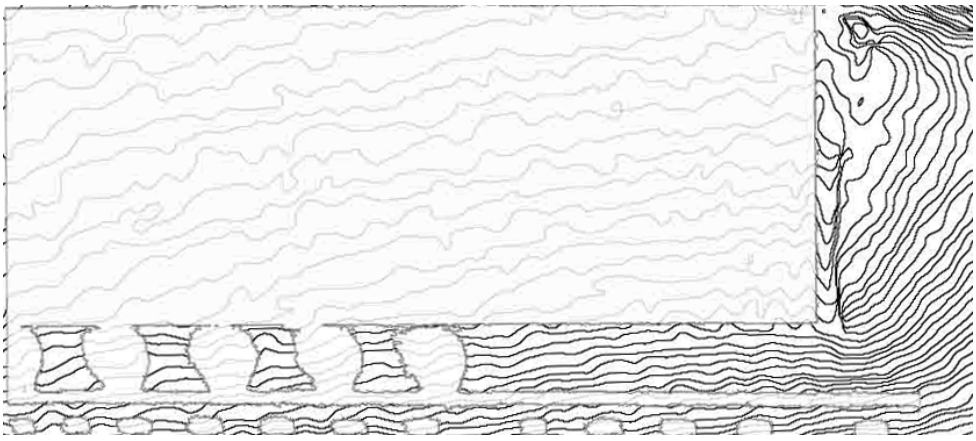


(a) U field

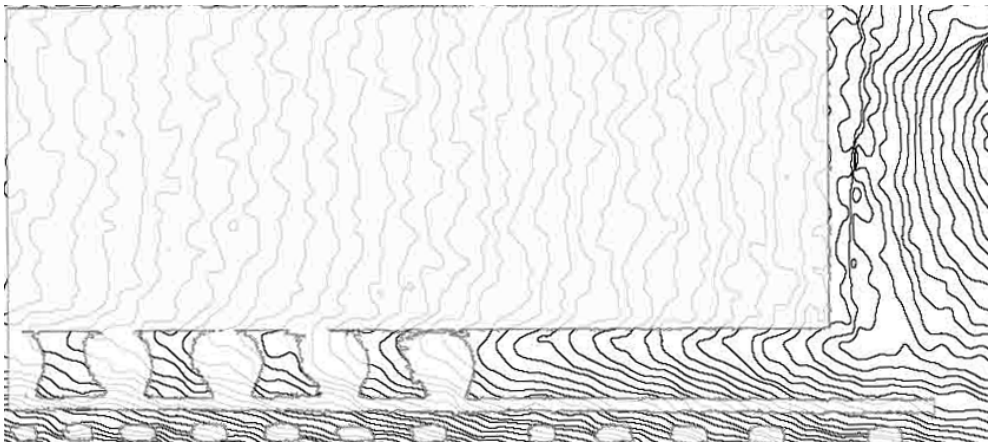


(b) V field

Figure 2.11: Phase maps for package without lid (a) U filed (b) V field with a resolution of 26nm/fringe



(a) U field



(b) V field

Figure 2.12: Phase maps for package with lid (a) U filed (b) V field with a resolution of 26nm/fringe

These phase maps were evaluated by the moiré analysis software to determine the displacement and strain distributions in the flip-chip package based on Eq. 2.5. Strain analyses were carried out along the three lines: the silicon-solder interface (Line A), the centerline of solder bumps (Line B) and the solder-substrate interface (Line C), as drawn in Figure 2.13.

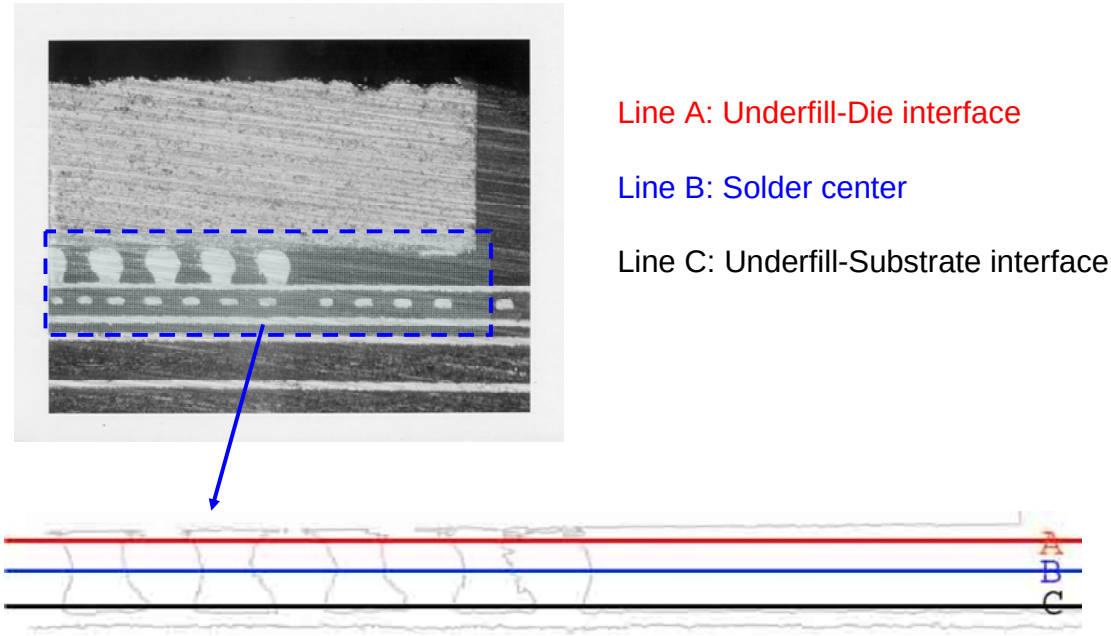
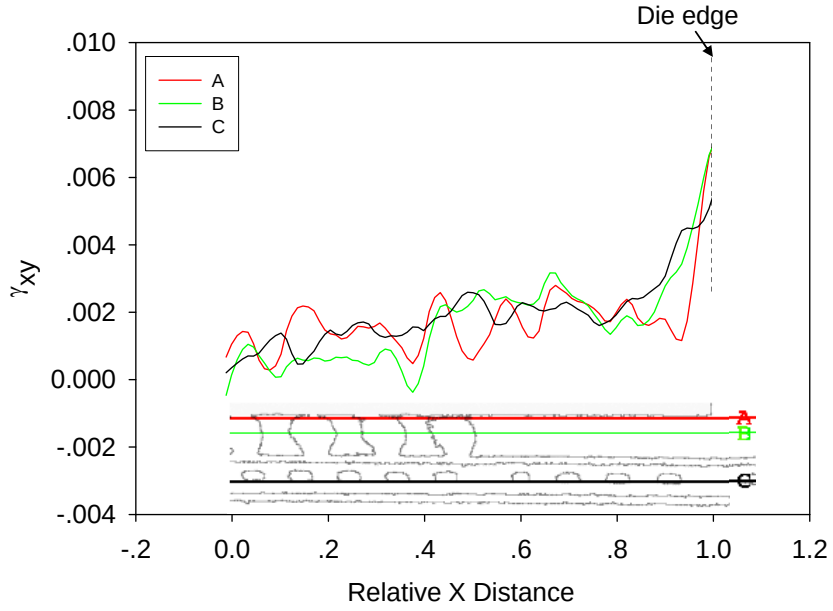


Figure 2.13: Region of interest for strain analysis

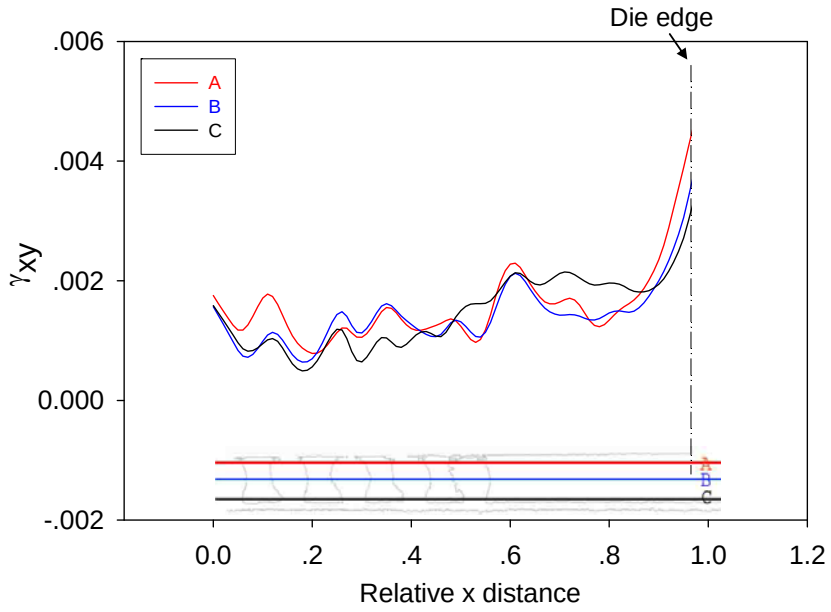
Shear strains are plotted along lines A, B, and C for both packages in Figure 2.14 (a) and (b). Several useful observations can be made from these diagrams. First, the shear strains along all three lines increase as the die edge is approached and reach a maximum at the die corner. Therefore the die corner area clearly has the largest shear strain and stress concentration and is more prone to underfill delamination failures. This problem will be discussed in Chapter 3. Second, the maximum shear strain of the package without lid is more than 1.5 times larger than that of the package with lid. This is to be expected since the overall bending of the lidless package is much larger.

The results from regular and high resolution moiré tests revealed that the package deformation induced by CTE mismatch can be reduced by applying a lid on top of the package. The CTE of the lid material is usually very close to that of the substrate; therefore it can cancel a good portion of the bending of the substrate. For both packages,

the die corner is identified as the critical region for mechanical stability due to the large strain concentration there. In comparison, the strain concentration is aggravated for the package without lid due to its large warpage. Without the support of the lid, the mismatch in the thermal deformation between the die and substrate is exerted on the solder and underfill buffer layer only, resulting in larger thermal deformation in this layer which may induce failure in solder joints, interfacial delamination between underfill and Si die, etc. during assembly and subsequent reliability tests [9-19]. Therefore, the mechanical reliability issues of flip-chip packages without lid are more critical and will be discussed in details in chapter 3 and 4.



(a)



(b)

Figure 2.14: Shear strain distribution for Package (a) without lid, and (b) with lid

2.4 Summary

In this chapter, the regular and high-resolution moiré interferometry was used to investigate the thermal deformation of flip-chip packages with organic substrates. The results demonstrated that the phase-shift moiré interferometry is a powerful technique for quantitative analysis of thermal deformation and strain distribution for high-density electronic packages. The high-resolution moiré interferometer has the capability of mapping local deformation to a resolution of 26nm as well as measuring strain distribution at small features [2-6]. The experimental results showed that the die corner was the most critical region in the package in terms of mechanical reliability. A comparison between packages with and without lid was conducted and a significant reduction of bending and strain level in the package was achieved by adding a lid on top

of the package to restrain the thermal deformation. Results from moiré interferometry tests can also provide data for verifications of FEA models for thermo-mechanical reliability studies of flip-chip packages which will be discussed in Chapter 4.

Chapter 3: Effects of Underfill Materials on Chip-Level and Package-Level Reliability

3.1 Introduction

Flip-Chip packaging technology is widely used now for advanced integrated circuits (IC). The introduction of C4 bumps as electrical connections between Si die and organic substrate provides high input/output (I/O) pad counts and improves electrical performance. In flip-chip packages, C4 bumps also serve as mechanical joints between the die and substrate and thus couple the deformation from the package substrate to the Si die. Large thermal deformation is commonly observed in the solder joints, which can be attributed to the CTE mismatch between the Si die and the organic substrate. This raises serious mechanical reliability concerns particularly for the outermost solder joints where the deformation reaches its maximum in flip-chip packages [1-3, 5].

Underfill is commonly employed to improve the solder joints reliability because it can couple the CTE mismatch among chip, solder, and substrate and effectively reduce the thermal stresses in the solder bumps. But even with the incorporation of the underfill, the solder reliability remains a significant concern [6] and new problems have emerged in flip-chip packages. The problems can be traced to the large bending in the package board together with large stresses at the die corners, both of which can lead to delamination at the passivation layer-to-underfill interface [3, 7]. Such stresses can also be coupled into the ultra low-k interconnects to drive delamination in the low-k layers especially when porous low-k dielectrics are incorporated [7-9]. In addition, the use of fine-pitch solders makes the underfilling and flux cleaning process more difficult, which may lead to void

formation and localized underfill delamination [10]. Several failure modes for flip-chip packages have been reported [3-13], including fatigue failure in bulk solder during thermal cycling, delamination at the intermetallic compound (IMC) layer due to overstress, underfill to die-passivation delamination and ultra low-k delamination at the die corners due to stress concentration. These failure modes are catalogued in Figure 3.1.

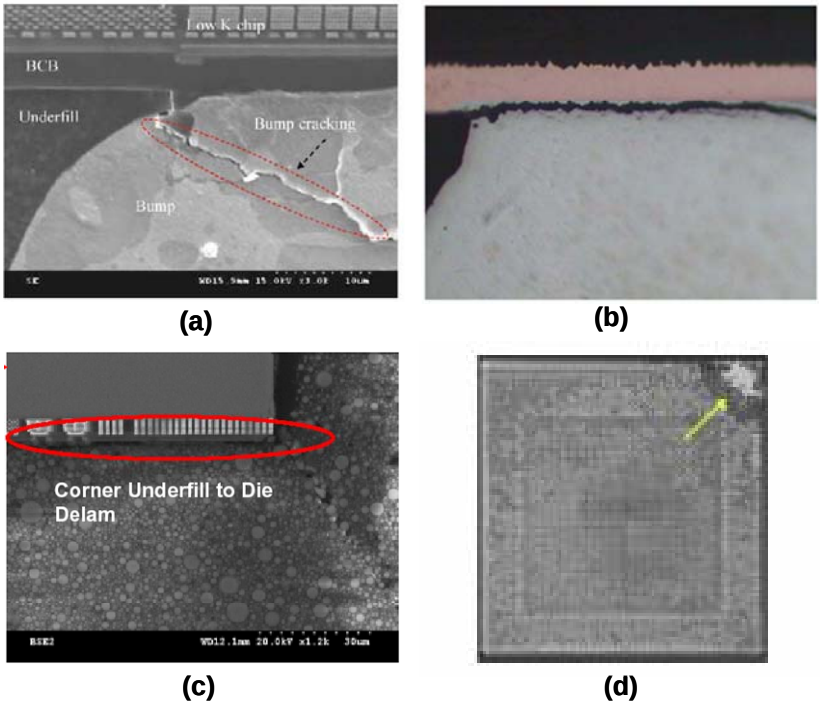


Figure 3.1: Common failure modes observed for flip-chip packages (a) bump cracking [3] (b) failure at IMC layer [7] (c) delamination of underfill at die corner [9] (d) ultra low-k dielectric delamination [11]

One way to reduce low-k delamination risk is to select underfills that are mechanically more compliant. However, increasing compliance of underfill contradicts the original purpose of underfill as a solder protection layer. It is clear that a proper choice of underfill has to meet a number of requirements to balance between solder joint

reliability and ultra low-k dielectrics integrity. These include good protection for both low-k materials and solder bumps, good adhesion to the passivation layer and solder mask, short filling time, minimum filler settlement and low moisture absorption. Previous studies by Chen et al. [3], Liu et al. [12], and Bansal et al. [13] found that a proper selection of underfill materials can significantly improve the mechanical reliability of flip-chip packages. Ong et al. [14] proposed an underfill selection methodology that ranked underfill materials based on three factors: adhesion performance, flowability, and underfill's thermomechanical properties.

With the implementation of fine-pitch Pb-free solder bumps and ultra low-k dielectrics in flip-chip packages, the requirements of underfill to provide good protection for both the solder joints and low-k dielectrics make underfill selection to be more difficult. Thus the underfill selection methodology has to be re-examined. In this chapter, the effects of thermo-mechanical properties of underfill on package reliability are investigated using moiré interferometry and finite element analysis (FEA). Several failure modes are analyzed, including solder thermal fatigue, Chip/underfill delamination, and low-k/passivation delamination. Underfill material is simulated as a two-stage Young's modulus (E) and CTE model which represents a realistic behavior of polymer materials. Darveaux's strain energy density model [15] is adopted to study the thermal fatigue behavior of Pb-free solder joints under thermal cycling. Sub-modeling technique and MVCC technique are used to calculate the interfacial delamination driving forces for underfill and low-k dielectrics. The effects of glass transition temperature (Tg), E, and CTE on solder fatigue, Chip/underfill delamination, and low-k/passivation delamination

are investigated using virtual underfill properties. Underfill selection for optimal reliability performance at both package level and chip level are discussed.

3.2 Effect of underfill on thermo-mechanical deformation of flip-chip packages

Moiré interferometry technique was employed to measure the thermo-mechanical deformations in flip-chip packages. Two packages with an identical structure except the underfill materials were tested. Package A contained an underfill with Tg of 150ºC while package B had an underfill with Tg of 70ºC. The underfill properties are listed in Table 3.1.

Table 3.1: Underfill mechanical properties

Underfill	**A**	**B**
Tg (^{o}C)	150	70
Young's Modulus (GPa)	4	8
CTE (ppm/^{o}C)	45	32

Both packages were built with a 40mmx40mm organic substrate and a 15mmx15mm Si die with a heat spreader on top as shown schematically in Figures 3.2 and 3.3. A 1200 lines/mm grating was applied to the cross-sectioned surface at three elevated temperatures and then cooled down to the room temperature, yielding three different thermal loads of -60ºC, -80ºC and -100ºC. Figure 3.4 shows the regular (i.e. non-high resolution) moiré images of both packages under thermal load of -100ºC with resolution of 417nm/fringe. The fringe density in package A was found to be higher than that in package B, indicating a larger overall deformation in package A. Die warpages under three thermal loads were analyzed and compared in Figure 3.5. For -60ºC thermal

load (from 82ºC to 22ºC), the die warpage in both packages was similar and the Tg effect was not observed. Therefore at this level of thermal load, the different E and CTE for these two underfills yielded little effect on package warpage. With the thermal load increased to -100ºC (from 122ºC to 22ºC), the die warpage of package A was significantly larger than that of package B, indicating a larger chip to substrate coupling in package A.

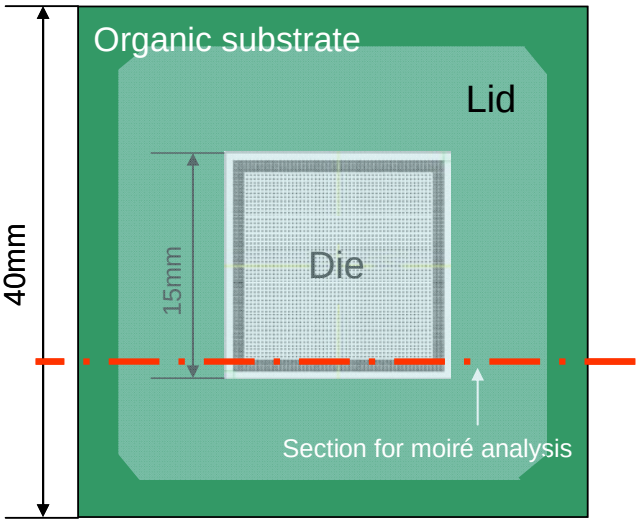


Figure 3.2: Schematic of flip-chip packages

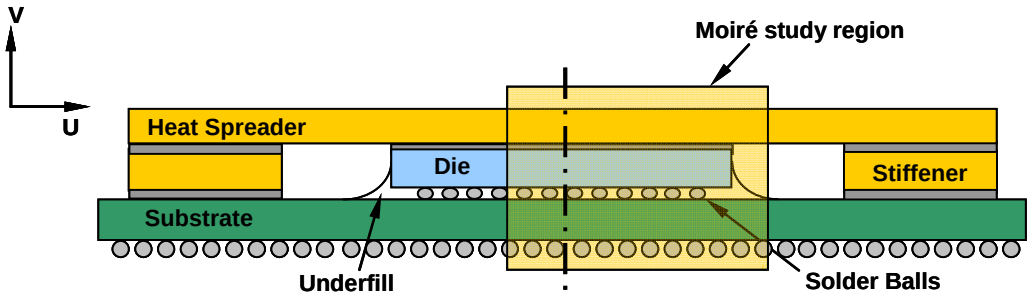
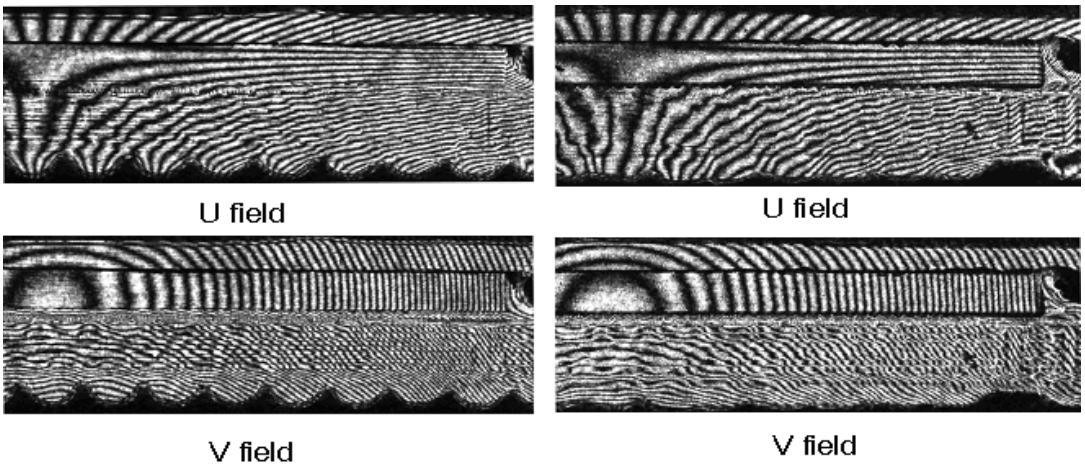


Figure 3.3: Cross-section view of flip-chip packages



(a) (b)

Figure 3.4: Regular moiré images of (a) package A and (b) package B, under thermal load of -100ºC

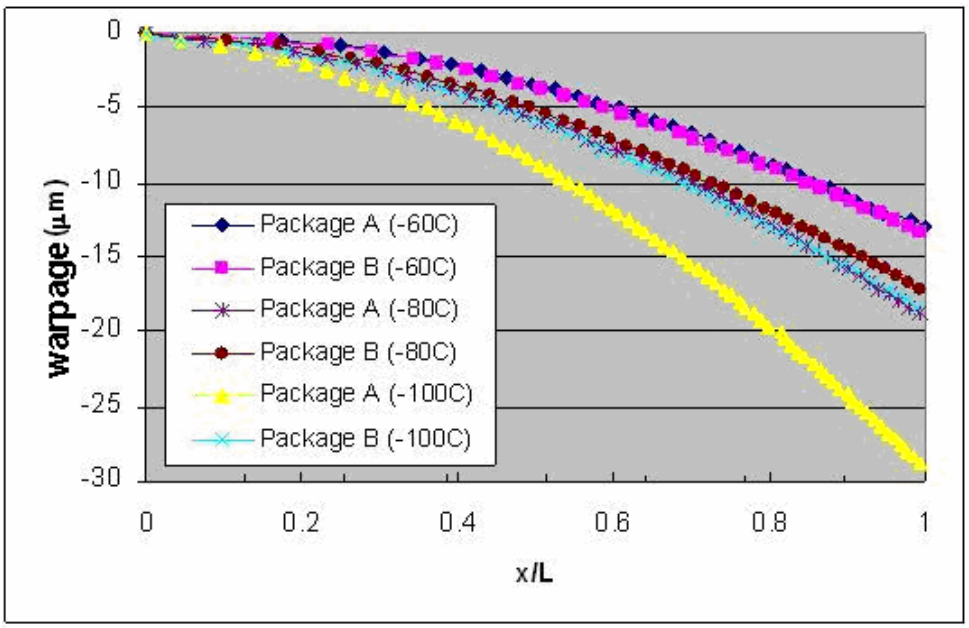


Figure 3.5: Comparison of die warpage for package A and B, at thermal loads of -60, -80, and -100 ºC

The thermal strain distribution in the underfill was investigated using the high-resolution moiré interferometry method. Figure 3.6 shows the U and V phase maps for package B under a thermal load of -60ºC. These phase maps were used to deduce the displacement and strain distributions in the flip-chip package along 3 lines: the silicon-solder interface (Line A), the centerline of solder bumps (Line B), and the solder-substrate interface (Line C), as shown in Figure 3.7. The shear strain distributions for both packages are displayed in Figure 3.8. The shear strain was found to increase from the die center to die edge and reach maximum at the edge. Overall, the shear strains in package B were larger than that of package A, especially in the middle of the underfill layer, because underfill B was more compliant at elevated temperatures.

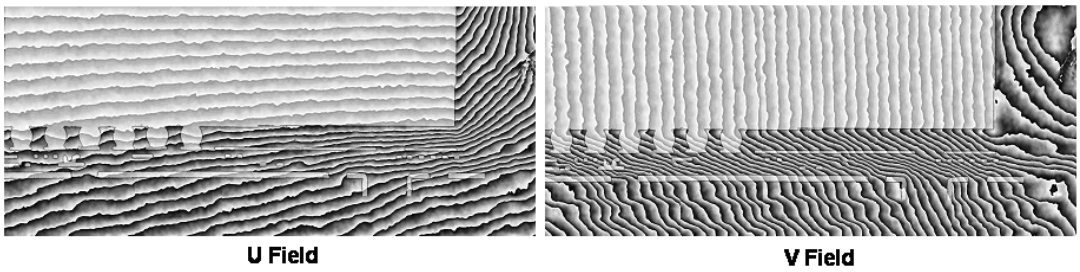


Figure 3.6: Phase map of package B obtained from high resolution moiré technique

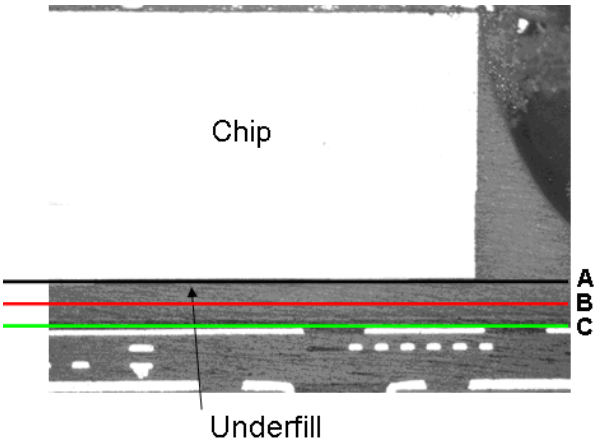
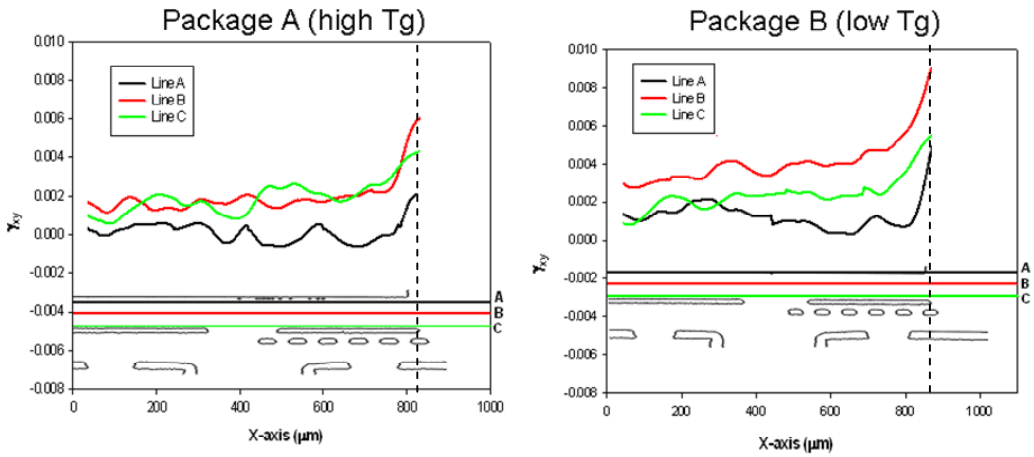


Figure 3.7: Microscopic picture showing strain analysis location, line A, B, and C



(a) (b)

Figure 3.8: Shear strain distribution for (a) Package A (b) Package B

3.3 Stress Analysis with finite element method (FEM)

Thermal stresses generated during the assembly process and subsequent thermal test raises serious reliability concerns for flip-chip packages. A qualified underfill should provide low stresses not only in the solder joints but also in the low-k interconnects. Of particular interest is the stress distribution in the package after underfilling. A FEA model shown in Figure 3.9 was developed in this study to simulate the thermo-mechanical

behavior of flip-chip packages with underfill. Due to the symmetry of the package, one quarter model with symmetric boundary condition was used. The dimension of the solder pitch in the model was 0.2mm. The material properties used in the model are listed in Table 3.2.

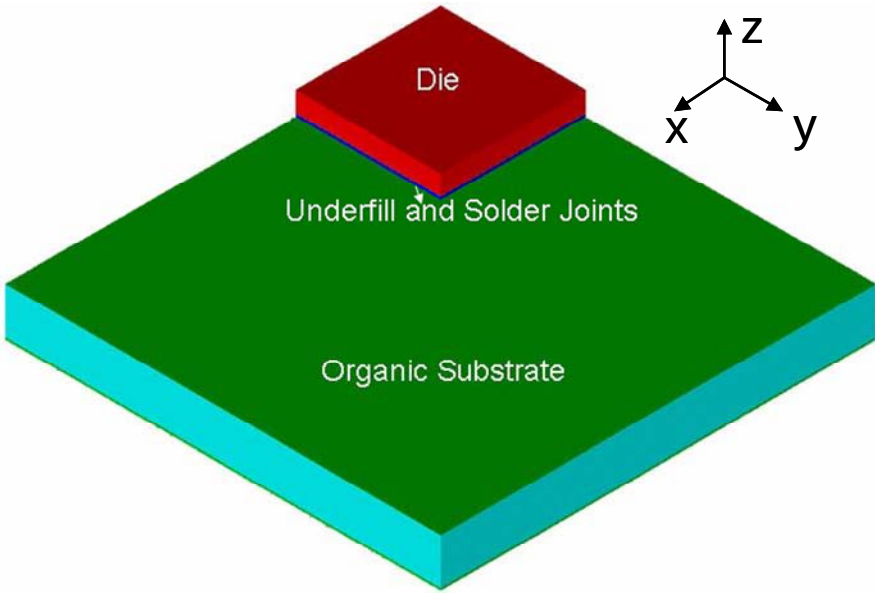


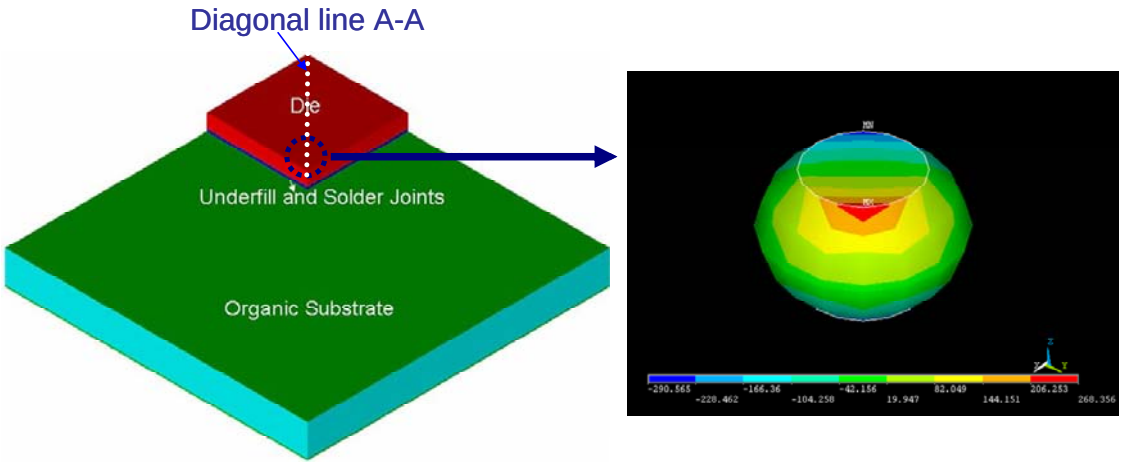
Figure 3.9: A quarter model of a flip-chip package

Table 3.2: Material properties used in the FEA model

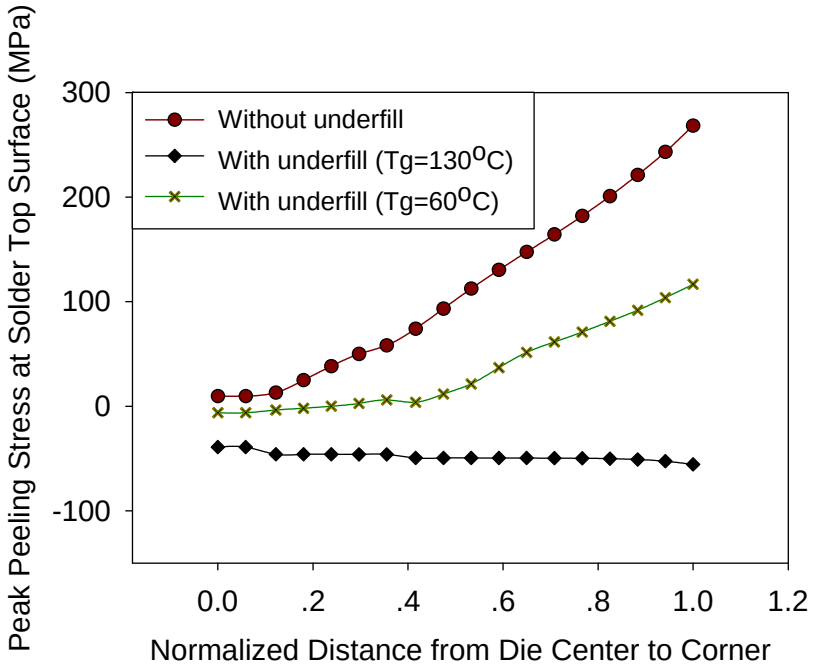
Material	Young's Modulus (GPa)	Poisson's ratio	CTE (ppm/^{o}C)
Si die	162	0.28	2.6
Pb-free Solder	88.53-0.142*T	0.40	21.5
Substrate	Anisotropic elastic properties		14 (in plane) 64 (out of plane)
Underfill	5.4 (T<Tg) ~0(T>Tg)	0.40	40 (T<Tg) 100 (T>Tg)

The thermal cycling process was simulated by applying a thermal load from 125^{o}C to -55^{o}C. The mechanical behavior of polymeric underfill was assumed to depend on two-stages of temperature dependent properties, one below Tg and the other above Tg. The stress distribution inside the solder joints and underfills were calculated by the FEA model. First package without underfill was investigated. Figure 3.10(a) shows a contour map of normal stress along the z-axis direction in the corner bump in this case. The stress distribution illustrated that upon cooling; there is a transition from compressive stress at its bottom surface to tensile stress at the top surface. This stress transition is a result of the distortion in the solder joint induced by CTE mismatch between the silicon die and the polymer substrates. The peeling stress σ_{zz} at the top surface, which is transferred into the silicon die via solder UBM and pad structure and is harmful to the silicon passivation layer and also to the BEOL low-k interconnects inside chip. However, the stress level in the solder bumps can be reduced when underfill material is incorporated. Figure 3.10(b) shows the effect of underfill on the maximum peeling stress in each solder along the diagonal line A-A of the die in Figure 3.10(a) for underfills with different Tg. First a significant drop in the peeling stress in solder bumps was found with implementation of the underfill epoxy. The results also showed that the higher the Tg of underfill, the lower the peeling stress. In contrast to the beneficial effect of underfill on the peeling stress, the introduction of underfill generates a high shear stress at the die corner, which is a potential threat for underfill to delaminate from silicon at the die corner. The Tg of the underfill plays an important role in controlling the shear stress level in a manner opposite to the peeling stress level, as shown in Figure 3.10(c). The maximum shear stress at the underfill/die interface increases by nearly 100% when the

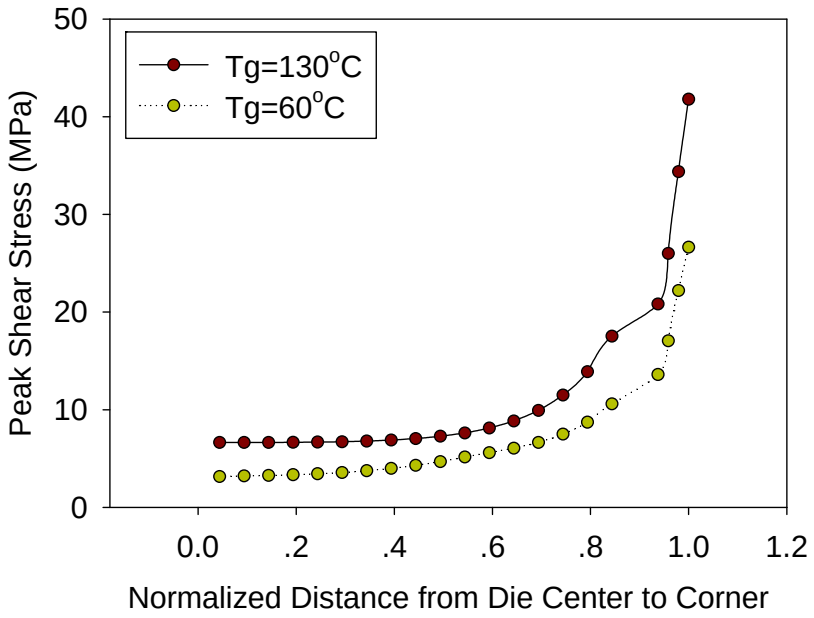
Tg of underfill increases from 60°C to 130°C. Underfill with higher Tg yields even larger shear stresses in the package.



(a)



(b)



(c)

Figure 3.10: Calculated stress distributions along diagonal line A-A of the die: (a) normal Z-stress in solder, (b) maximum peeling stress at solder top surface and (c) shear stress at underfill/die interface at the die corner

3.4 Thermal Cycling Fatigue Reliability of Pb-free Solder Bumps

The low-cycle fatigue life of solder bumps has been extensively studied by thermal cycling tests at elevated temperatures [15-20]. Such accelerated fatigue tests are time-consuming often requiring weeks or even months to collect one set of data. Besides, direct observation of fatigue crack initiation and propagation during cyclic tests is very difficult. Therefore simulation methods have been widely used to study the solder fatigue behavior. Several solder joint fatigue life prediction models have been proposed based on

various stress, strain and fracture criteria [15, 20]. One of the most popular approaches is an energy-based method proposed by Darveaux [15]. In Darveaux's model the inelastic strain in solder joints during thermal cycling consists of two parts, a time-dependent creep strain and a time-independent plastic strain.

$$\varepsilon_{in} = \varepsilon_c + \varepsilon_p \qquad (3.1)$$

The creep strain behavior of solder joints can be expressed as follows:

$$\varepsilon_c = \frac{d\varepsilon_s}{dt} t + \varepsilon_T (1 - \exp(-B \frac{d\varepsilon_s}{dt} t)) \qquad (3.2)$$

$$\frac{d\varepsilon_s}{dt} = C_{ss} [\sinh(\alpha\sigma)]^n \exp(\frac{-Q_a}{kT}) \qquad (3.3)$$

where $\frac{d\varepsilon_s}{dt}$ is the steady state strain rate, ε_T is the transient creep strain, B is the transient creep coefficient, k is Boltzmann's constant, T is the absolute temperature, σ is the applied stress, Q_a is the apparent activation energy, n is the stress component, α is the break-down stress level based on a power law form, and C_{ss} is a constant.

The plastic strain component is described by the following strain hardening relationship:

$$\varepsilon_p = C_p (\frac{\sigma}{G})^{m_p} \qquad (3.4)$$

where ε_p is the time-independent plastic strain, G is the shear modulus, C_p and m_p are constants.

To apply Darveaux's model, a constitutive relationship representing the elastic-plastic behavior of the solder joint is required. A commercial FEM package, Ansys, has

viscoplastic elements available which use Anand's constitutive model [19]. Anand's model consists of a flow equation and three evolution equations:

Flow Equation

$$\frac{d\varepsilon_p}{dt} = A[\sinh(\xi\sigma / s)]^{1/m} \exp\left(\frac{-Q}{kT}\right) \qquad (3.5)$$

Evolution Equation:

$$\frac{ds}{dt} = \{h_o(|B|)^{\alpha} \frac{B}{|B|}\} \frac{d\varepsilon_p}{dt} \qquad (3.6)$$

where $B = 1 - \frac{s}{s^*}$

$$s^* = \hat{S}\left[\frac{d\varepsilon_p / dt}{A} \exp\left(\frac{Q}{kT}\right)\right]^n \qquad (3.7)$$

where Q is activation energy, k is Boltzmann's constant, A is pre-exponential factor, ξ is multiplier of stress, m is strain rate sensitivity of stress, s is the deformation resistance, h_o is hardening constant, $\hat{S}$ is the coefficient for deformation resistance saturation value, n is strain rate sensitivity of saturation (deformation resistance) value, α is strain rate sensitivity of hardening.

The constants for Anand's model for both lead and lead-free solder are listed in Table 3.3 [6, 15, 21].

Table 3.3: Constants for lead and lead-free solder in Anand's model

Anand model constants for leaded and lead-free solders

Variable \ Solder	Sn36Pb2Ag[7]	Sn4Ag0.5Cu /Sn3.4Ag0.8Cu [10]
s_o (MPa)[1]	12.41	1.3
Q/R (1/K)	9400	9000
A(1/s)	4e6	500
A	1.5	7.1
M	0.303	0.3
h_o (MPa)	1379	5900
$\hat{s}$ (MPa)	13.79	39.4
N	0.07	0.03
A	1.3	1.4

[1] S_0 is the initial value of deformation resistance

For this calculation, a typical slice model was built as shown in Figure 3.11. Two thermal cycles were simulated in order to establish a stable stress-strain hysteresis loop. The strain energy density accumulation per thermal cycle within the "critical" solder bump is calculated. The strain energy density is related to the crack initiation and growth lifetime as follows:

$$\text{Crack initiation: } N_o = K1\,\Delta W_{ave}^{\ K2} \qquad (3.8)$$

$$\text{Crack growth: } \frac{da}{dN} = K3\,\Delta W_{ave}^{\ K4} \qquad (3.9)$$

$$\Delta W_{ave} = \frac{\sum \Delta W * V}{\sum V} \qquad (3.10)$$

where K1 to K4 are constants depending on solder materials and modeling methodologies. ΔW_{ave} is the average viscoplastic strain energy density accumulated per cycle for the elements at the die/solder interface, ΔW is the strain energy density accumulated per cycle of each element and V is the volume of the slice element.

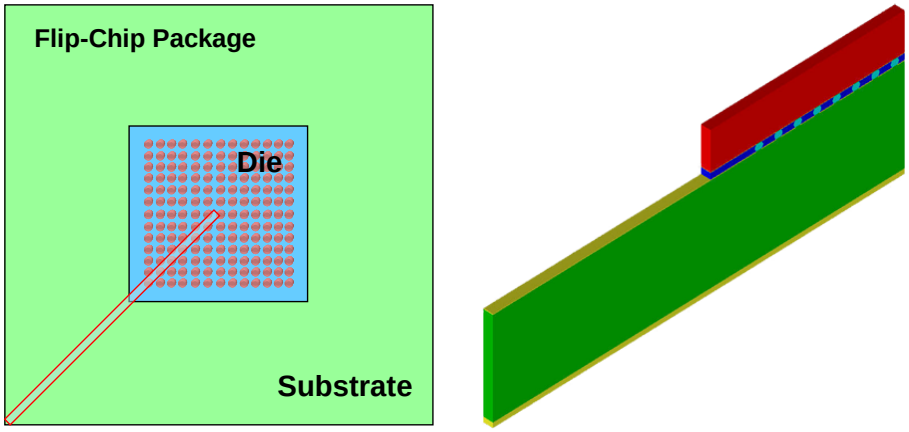


Figure 3.11: A schematic slice model used for solder fatigue study

3.4.1 Role of underfill properties

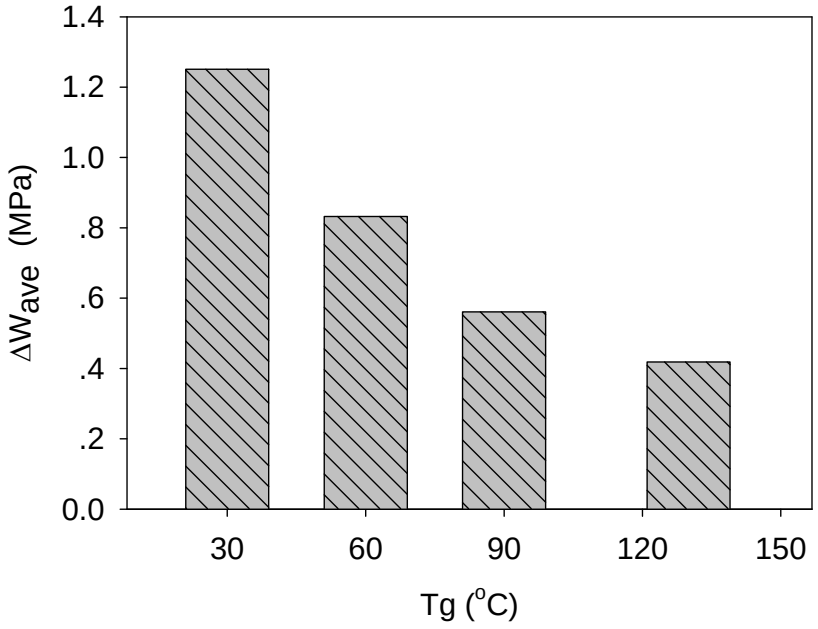
In a previous study, the thermal fatigue life time of solder joints was found to decrease with increasing strain energy accumulated ΔW_{ave} [16, 22]. Therefore in this dissertation, we investigated the effect of the thermo-mechanical properties of underfill on solder fatigue life by calculating the change in the accumulated strain energy, ΔW_{ave}, during thermal cycling tests. For this purpose, the effect of Tg, E, and CTE on the thermal cycling reliability of lead free solder bumps was investigated. Different combinations of these parameters were used so that not only the effect of their combinations but also the effect of the individual parameters can be examined. The

objective is to identify the most critical property for improving solder fatigue life. The results and the properties of the underfills used in this study are described below:

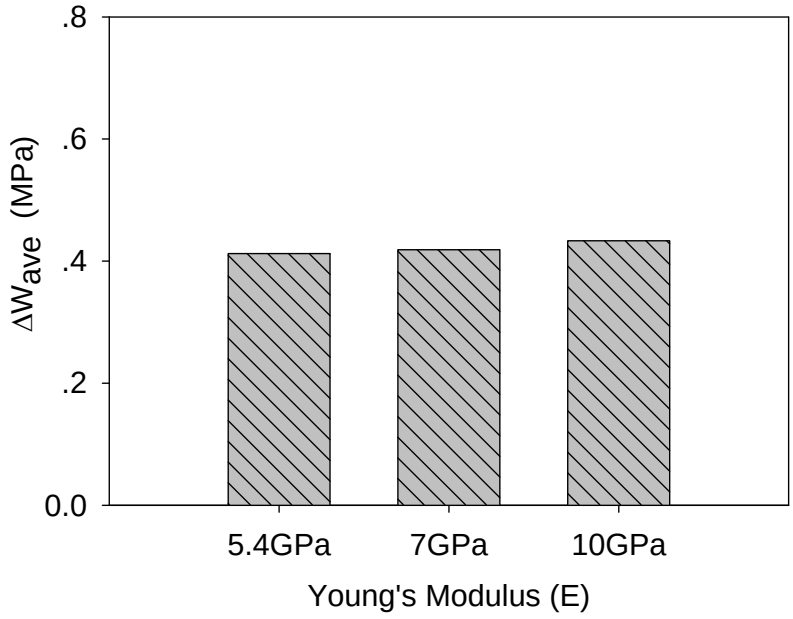
Tg effect: To separate the Tg effect from the other two parameters, four underfills with varying Tg but fixed E (7GPa) and CTE (30ppm/^{o}C) were studied. The Tg was varied from 30^{o}C to 130^{o}C as plotted in Figure 3.12(a). The averaged strain energy density accumulated per thermal cycle was found to decrease by a half when the Tg of underfill increases from 30^{o}C to 130^{o}C, indicating that with a higher Tg, the underfill is more effective in suppressing solder fatigue failure.

E effect: Similar to the Tg study, three underfills were studied which had a different E but fixed Tg (130^{o}C) and CTE (30ppm/^{o}C) as shown in Figure 3.12(b). Simulation results showed that E had little impact on the fatigue behavior of solder joints under thermal cycling.

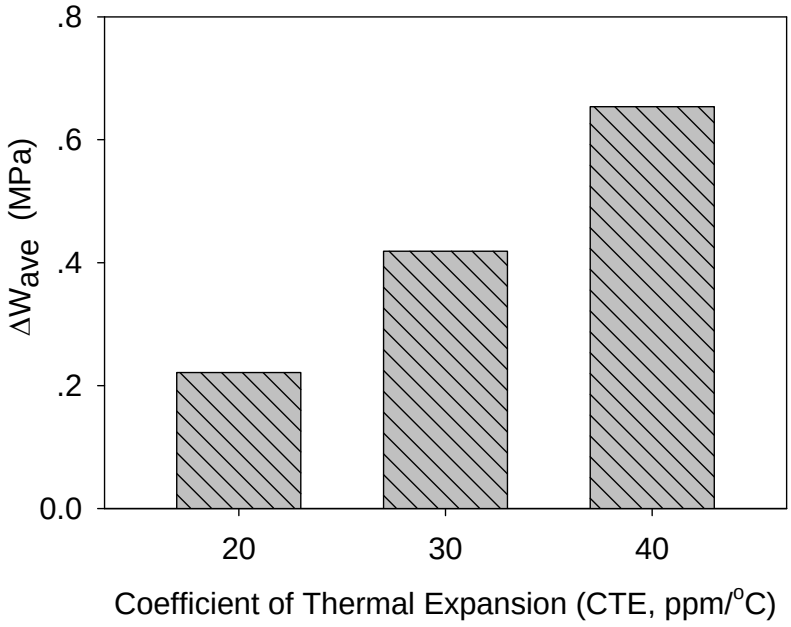
CTE effect: In the CTE case, three underfills with varying CTE of 20ppm/^{o}C, 30ppm/^{o}C, and 40ppm/^{o}C but fixed Tg (130^{o}C) and E (7GPa) were studied as in Figure 3.12(c). The calculated strain energy density showed that underfill with the highest CTE in the study, 40ppm/^{o}C, yielded the shortest fatigue life of solder joints. The results indicated that, in addition to the global CTE mismatch between the Si die and the plastic substrate, the local CTE mismatch between underfill and solder bumps is also important in determining the fatigue behavior of solder joints. Considering the CTE of solder bumps used in the model, 21.5ppm/^{o}C, the result showed that the underfill with CTE closer to that of the solder joints produced a better solder fatigue lifetime.


1.4
1.2
1.0
.8
.6
.4
.2
0.0
ΔWave (MPa)
30
60
90
120
150
Tg (°C)

(a)


.8
.6
.4
.2
0.0
ΔWave (MPa)
5.4GPa
7GPa
10GPa
Young's Modulus (E)

(b)



(c)

Figure 3.12: Effect of underfill properties on solder thermal fatigue behavior

3.5 Underfill delamination and Cu/low-k interconnect reliability

Besides the solder fatigue failure, underfill delamination and low-k dielectric fracture are two other failure modes that are often observed after packaging and reliability tests (Figure 3.1) [3, 23]. In order to study the packaging-induced crack driving force at these interfaces, structural details in both packages and solder bumps must be considered. However it is challenging to include all details in one model because of the dimensional difference in solder balls and the whole package. In order to study the problem, a sub-modeling technique was introduced to reduce the calculation to a manageable level. Figure 3.13 shows the sub-model that was developed to investigate the interfacial crack driving force at the relevant interfaces. Following the results of failure

analysis, initial cracks were inserted into the model as defects. The corresponding energy release rates for these cracks were calculated by the modified virtual crack closure technique. The details of sub-modeling technique and MVCCT will be described in chapter 4. The effects of Tg, E, and CTE on packaging reliability were investigated individually. The thermal load used in the study was -180ºC (from 125°C to -55°C).

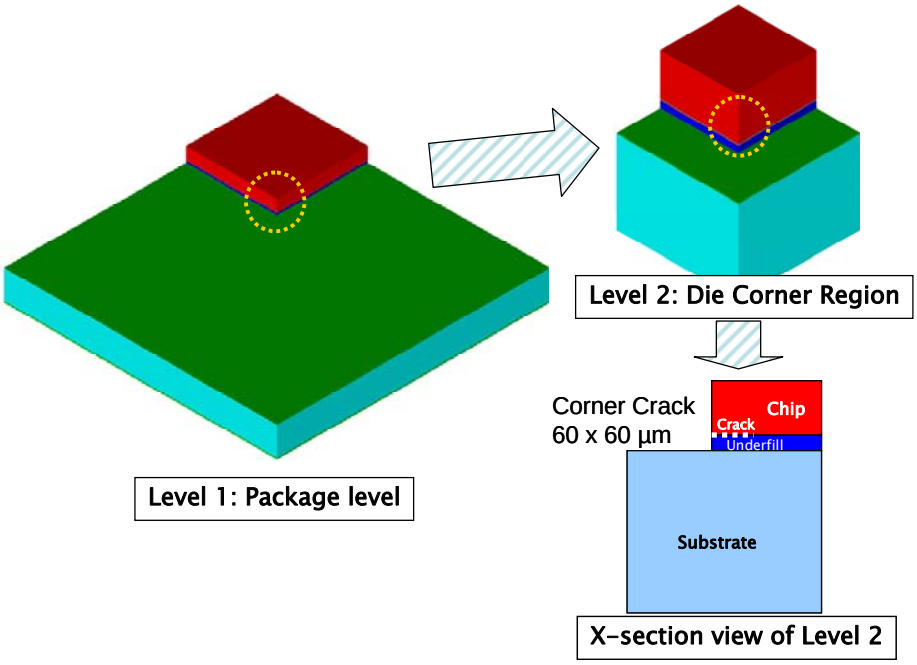
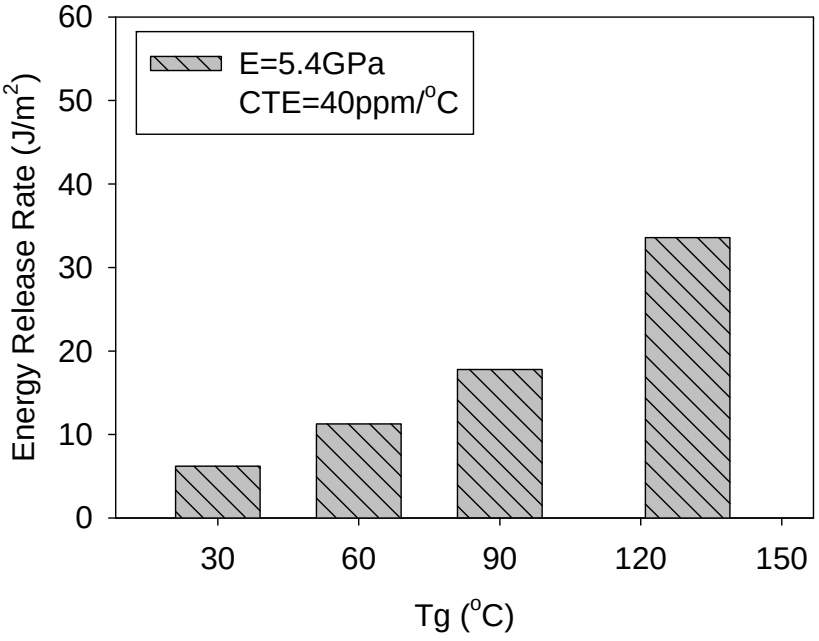


Figure 3.13: Hierarchical levels of sub-modeling to study chip/underfill delamination

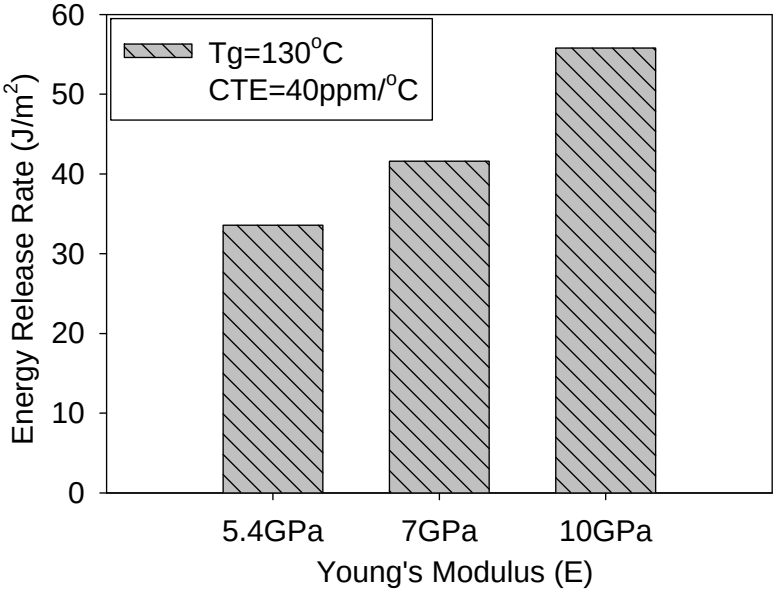
3.5.1 Underfill delamination

Energy release rate (ERR) of delamination at the chip/underfill interface was studied by using the same set of underfills as in the solder fatigue study. The calculated ERR data are plotted in Figure 3.14. The effect of Tg showed the opposite trend to that of solder fatigue. Underfill with high Tg yielded a larger crack driving force for underfill delamination due to the larger stress concentration at the die corner compared to that of low Tg underfill. Tg was found to be the key parameter in determining the crack driving

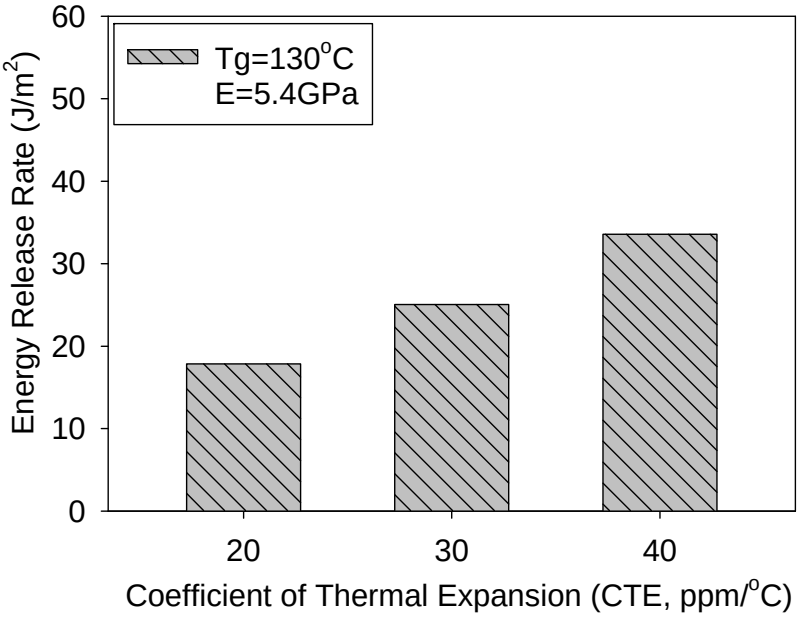
force. It's about 5.5 times difference in the ERR with Tg varying from 130^{o}C to 30^{o}C. E and CTE also play important roles in the chip/underfill delamination as demonstrated in Figure 3.14(b) and (c). ERR increased by 67% when the E of underfill increased from 5.4GPa to 10GPa and around 100% when CTE increased from 20ppm/^{o}C to 40ppm/^{o}C. By comparing this set of results with the results in Figure 3.12, it was concluded that increasing Tg of underfill provided better protection for solder joints from fatigue failure under thermal cycling but increased the hazard of underfill-to-chip delamination. Therefore E and CTE should be optimized instead of Tg in order to improve underfill reliability without impacting the solder integrity. Decreasing the E of the underfill can help reduce the ERR for chip/underfill delamination without impacting solder fatigue life because fatigue life time is determined by the creep and plastic deformation in the solder which is not very sensitive to E. In both cases, underfill with smaller CTE (~ 20ppm/^{o}C) yielded better reliability performance.


E=5.4GPa
CTE=40ppm/°C
Energy Release Rate (J/m2)
0
10
20
30
40
50
60
30
60
90
120
150
Tg (°C)

(a)


Tg=130°C
CTE=40ppm/°C
Energy Release Rate (J/m2)
0
10
20
30
40
50
60
5.4GPa
7GPa
10GPa
Young's Modulus (E)

(b)



(c)

Figure 3.14: Effect of underfill properties on chip/underfill delamination (a) Tg effect (b) E effect (c) CTE effect

3.5.2 Cu/ultra low-k interconnect reliability

Another common failure for flip-chip packages is "white bumps" found in the C-Mode Scanning Acoustic Microscopy (C-SAM) test which denotes low-k delamination at the location (Figure 3.1(d)). The reliability issues caused by replacing fully dense low-k material with porous low-k and ultra low-k materials are gaining more attention due to their weak mechanical properties. The fracture resistance of porous low-k materials is usually in the range of 2~6 J/m^2, much weaker than adhesion strength of underfill to solder mask, which can be over 35 J/m^2 by adding silane additives to promote adhesion [24, 25]. Moreover, the dicing defects at the periphery of Si die can serve as initial

defects and facilitate the crack propagation [12]. Fracture and delamination in the low-k interconnect structure during thermal cycling were observed and reported by Chen et al. as shown in Figure 3.15 [3].

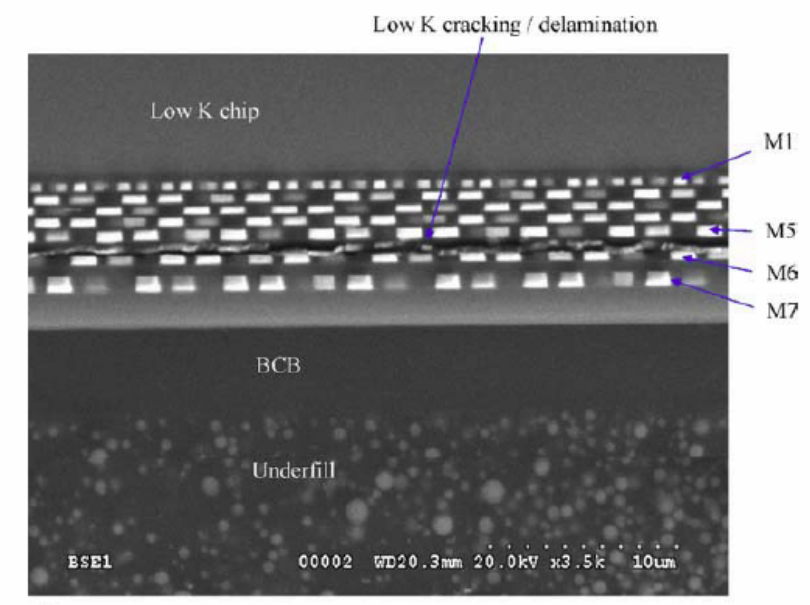


Figure 3.15: Low-k delamination in low-k layer [3]

To study the effect of underfill material on Cu/low-k interconnect reliability, a simplified interconnect structure with porous low-k layer was analyzed as shown in Figure 3.16. A pre-crack as labeled in the figure was inserted into the structure as an initial defect. The ERRs obtained for low-k layer delamination are summarized in Figure 3.17. Underfill mechanical properties were found to have a large effect on the low-k reliability, especially Tg. The ERR of low-k dielectric delamination can increase by 5 times when Tg of the underfill increases from 30^{o}C to 130^{o}C. E and CTE also impact the ERR values although the effect is not as significant as Tg. An increase in ERR of 66% and 33% was observed by varying E and CTE, respectively, as shown in Figure 3.17(b)

and (c). The results showed that for Cu low-k interconnects, underfills with lower Tg, smaller E and CTE are required to protect the low-k layer from delamination. In addition, underfills have to provide proper protection for solder bumps and prevent underfill delamination. These requirements leave a smaller selection window for a desirable range of mechanical properties of underfills. A comparison of crack driving force between different low-k materials was plotted in Figure 3.18. The dielectric material with a lower k value was found to induce larger driving forces for failure in the low-k layer. It was also noticed that for the given crack length, most of the ERR obtained are larger than the nominal fracture strength of low-k dielectrics which is about 2~6 J/m^2 [24], indicating an unstable crack propagation. As the technology node evolves into 32nm and 22nm, the choice of underfills is even more difficult due to the use of dielectric materials with lower dielectric constants and Pb-free solder bumps.

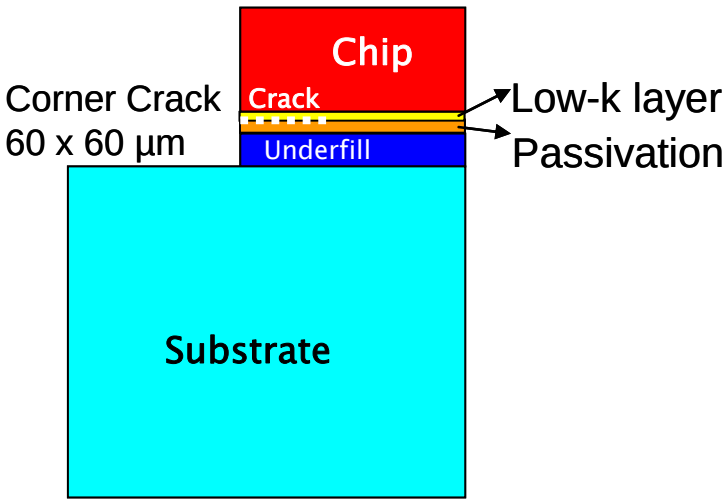
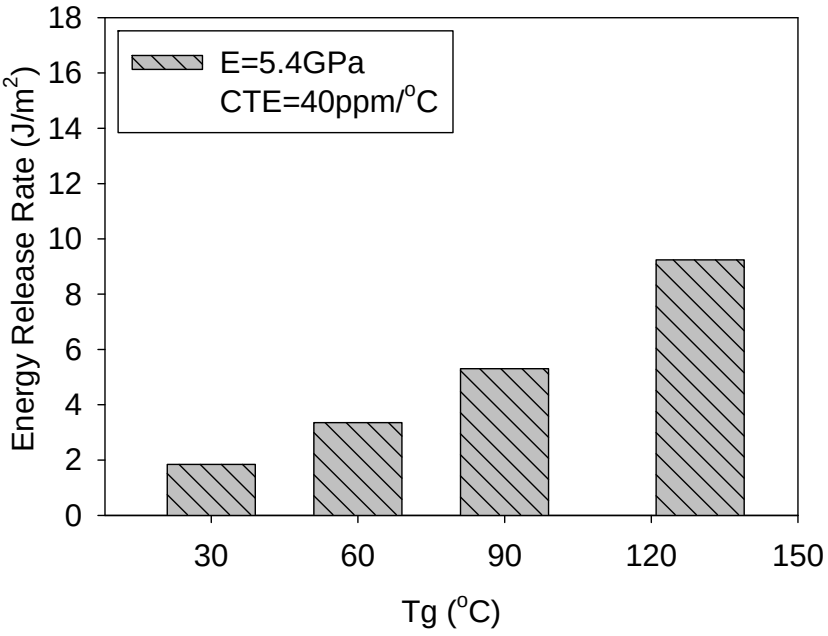
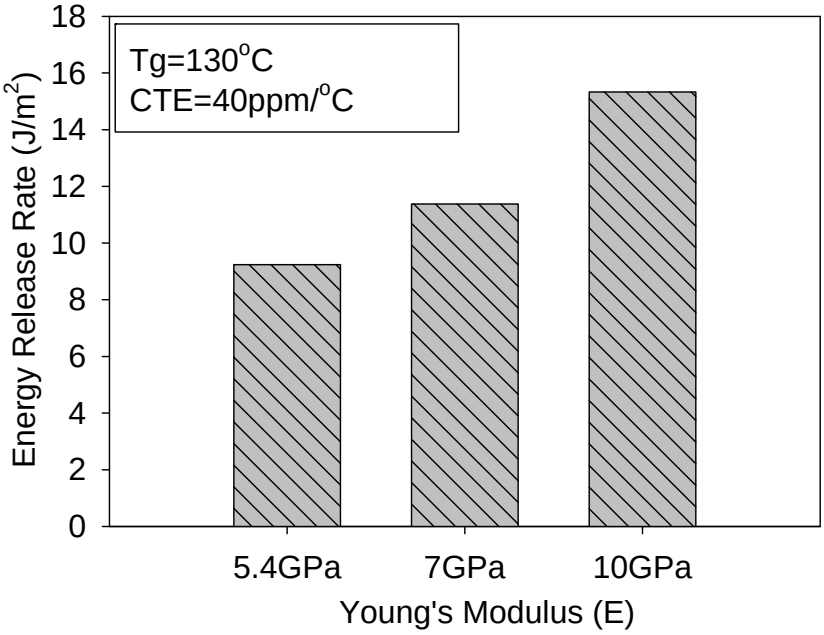


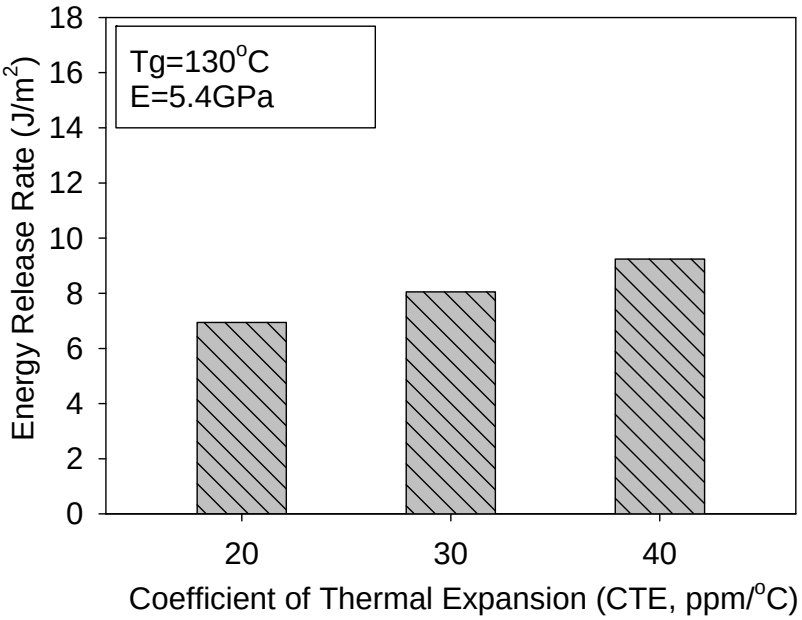
Figure 3.16: FEA model for low-k delamination study


E=5.4GPa
CTE=40ppm/°C
Energy Release Rate (J/m2)
0
2
4
6
8
10
12
14
16
18
30
60
90
120
150
Tg (°C)

(a)


Tg=130°C
CTE=40ppm/°C
Energy Release Rate (J/m2)
0
2
4
6
8
10
12
14
16
18
5.4GPa
7GPa
10GPa
Young's Modulus (E)

(b)



(c)

Figure 3.17: Effect of underfill properties on low-k layer delamination from passivation layer (a) Tg effect (b) E effect (c) CTE effect

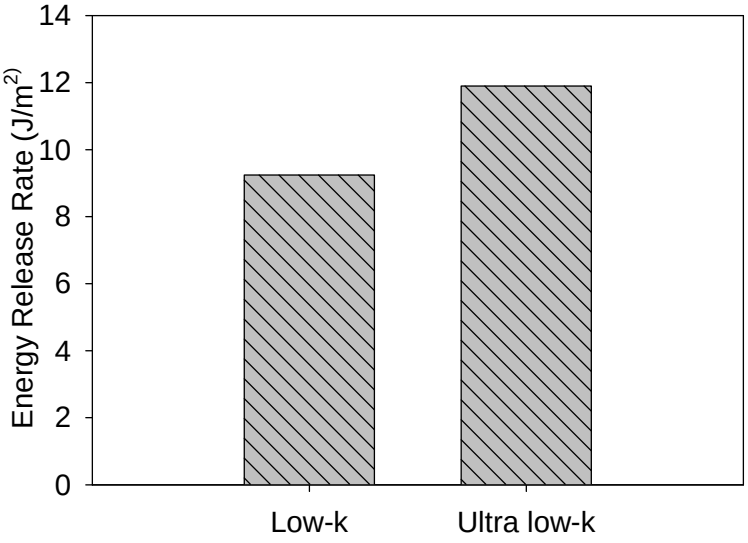


Figure 3.18: Comparison between different low-k materials

3.6 Adhesion study of underfill and moisture effect on underfill adhesion

In previous sections, the effects of material properties, like E, CTE, and Tg of underfill, on the driving force for fracture were studied. The energy release rate is defined as the amount of strain energy released per unit area of crack growth. On the other hand, the resistance to crack growth is the energy required to break the bonds, create new surfaces, and generate dislocations or other defects near the crack tip. The total energy required to grow the crack by a unit area is defined as the fracture toughness of the material. A fracture criterion is thus established by comparing the energy release rate with the fracture toughness [26]. If the driving force exceeds the interface adhesion strength, the crack will grow. Otherwise, the crack won't propagation. Therefore, study of the adhesion strength of underfill to other materials is of great interest. In this study, a double cantilever beam (DCB) method [27] was used to measure the interfacial fracture energy of underfill materials to Cu and solder resist (SR) films. These two interfaces are relatively weak and are the source of failure observed repeatedly in packages with Cu pillar structures. Delamination at underfill/solder resist interface may lead to failure in the solder joints eventually due to the crack propagation. The failure at the Cu pillar/underfill interface can create sharp cracks and pose high risk for fracture in low-k interlayer dielectrics (ILD) when the crack propagates into the die.

The DCB method measures the mode I adhesion strength between two materials by pulling the sample apart while monitoring the load and the opening displacement, etc. A pre-crack generated by Cu sputter or mold release can be built into the sample in order to initiate failure at desired interface. The sample scheme for the DCB test is shown in Figure 3.19.

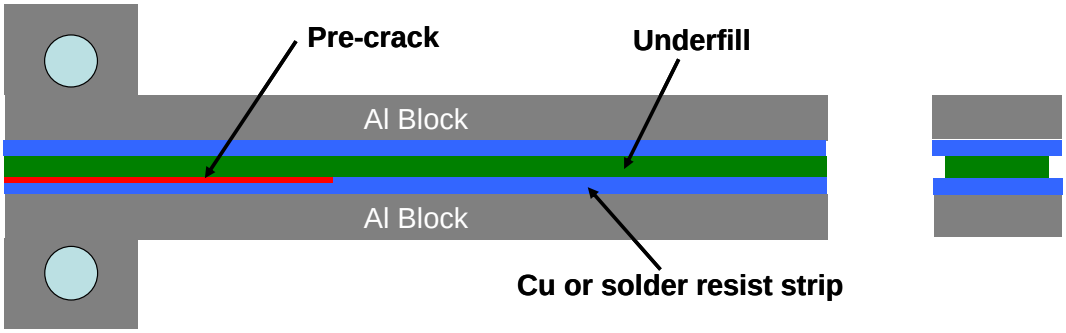


Figure 3.19: Sample scheme for DCB measurement

In our experiments, the Cu or solder resist films were attached to two aluminum end blocks by epoxy glue first and then an underfill layer was sandwiched between solder resist films or Cu strips by capillary action with a sharp pre-crack placed along the desired interface. An extended arm of the aluminum end block was used to reinforce the solder resist or Cu strip and prevent it from cracking during testing. The width of underfill layer was made narrower than the solder resist film, on purpose, to reduce the critical load required to fracture the specimen and also to prevent the solder resist edge flaws from interfering the interface fracture [28].

DCB samples were tested in a micro-tensile system at room temperature. Figure 3.20 shows a sample loading curve of DCB tests. The DCB sample was first loaded until the pre-crack started to grow, and then unloaded to obtain the sample stiffness at that point. This loading/unloading cycle was repeated until the sample failed. When the crack was not growing, the sample stiffness remained constant hence the loading/unloading curve was linear. Once the load reached a critical value, the loading curve started deviating from the previous unloading curve. The fracture toughness, Gc, was calculated

from the critical load for the crack to grow, the sample stiffness, and the geometry dimensions of the DCB samples [24].

The first interface studied was the Cu to underfill interface. Figure 3.20 shows the fracture energy of this interface measured at ambient condition. The mean value of the adhesion strength is close to 8.6 J/m^2.

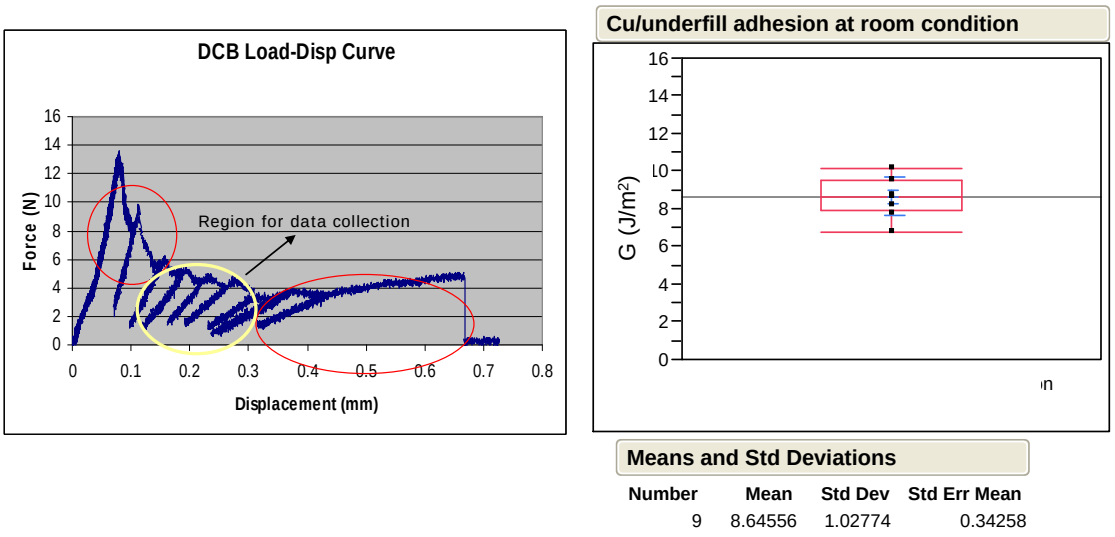


Figure 3.20: Fracture resistance of Cu/underfill interface at room condition

XPS surface analysis at both Al beams of the tested sample verified that the delamination occurred at the Cu/underfill interface instead of cohesion failure inside underfill as shown in Figure 3.21.

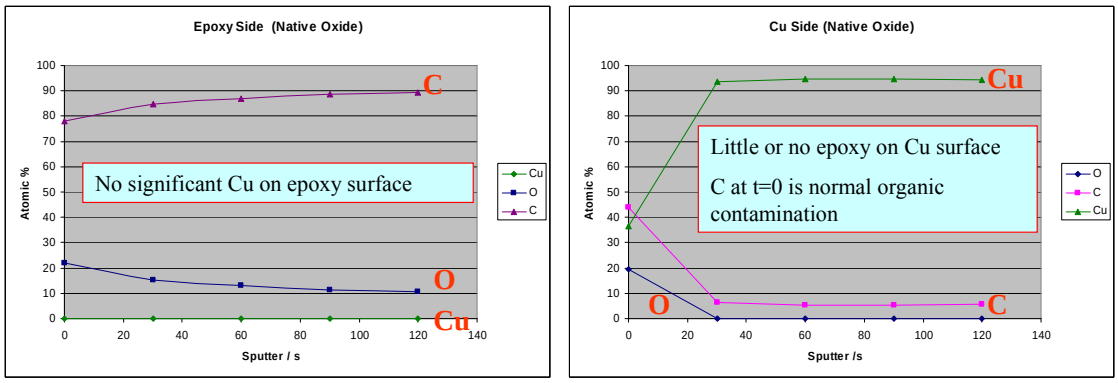


Figure 3.21: XPS surface analysis of tested Cu/underfill DCB samples

As mentioned above, these adhesion measurements were done at ambient condition in the lab. While in the daily usage, the microelectronic packages may be exposed to various moisture conditions. It has been reported that moisture plays an important role in the thermal and mechanical reliability of microelectronic packages, especially for underfill polymer materials which have high moisture diffusivities [28-30]. Therefore it is important to investigate the performance of the Cu/underfill interface at conditions with high moisture concentration. For this purpose, the DCB test samples after full assembly with Al block were soaked in a moisture chamber (85RH) at 85^{o}C for 5 days. After moisture absorption, these samples were tested at room temperature immediately to measure the adhesion strength at the interface. To understand the moisture diffusion and concentration in the soaked samples, FEA was employed to simulate the moisture absorption process as a function of time. Wong and Rajoo [29] proposed a method using a heat conduction equation built in the FEA software to simulate the moisture diffusion. A comparison between these two approaches is given in Table 3.4.

Table 3.4. Thermal diffusion vs. moisture diffusion

Properties	Thermal	Moisture
Field variable	Temperature,T	$w= C/C_{sat}$
Density	ρ (kg/m^3)	1
Conductivity	k $(W/m\ ^0C)$	$D * C_{sat}$ $(kg/sec\ m)$
Specific capacity	c $(J/kg\ ^0C)$	C_{sat} (kg/m^3)

Heat conduction

$$\frac{\partial T}{\partial t} = \alpha_T \left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2}\right)$$

Ficks' Diffusion Equation

$$\frac{\partial C}{\partial t} = D\left(\frac{\partial^2 C}{\partial x^2} + \frac{\partial^2 C}{\partial y^2} + \frac{\partial^2 C}{\partial z^2}\right)$$

where C is the moisture concentration, C_{sat} is the saturated moisture concentration, and D is the moisture diffusivity.

The moisture parameters used in the simulation are listed in Table 3.5. These parameters were obtained by moisture absorption and adsorption test as described in Lu's paper [28]. Figure 3.22 shows the FEA model for the moisture simulation including Al beam, Cu strips and underfill.

Table 3.5: Parameters for moisture diffusion simulation

Underfill tested	85C and 85RH
D (mm^2/s)	4.33E-06
C_{sat} (mg/mm^3)	1.10E-02
$D*C_{sat}$ (mg/s/mm)	4.76E-08

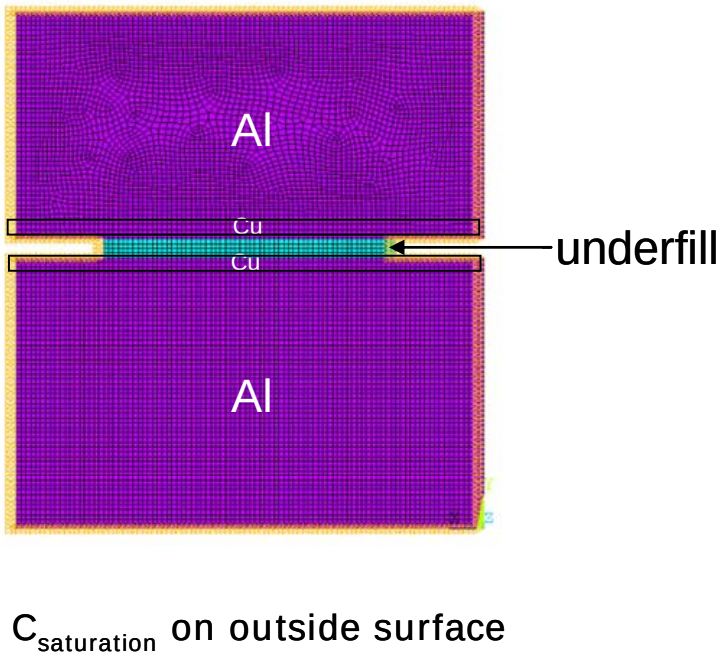
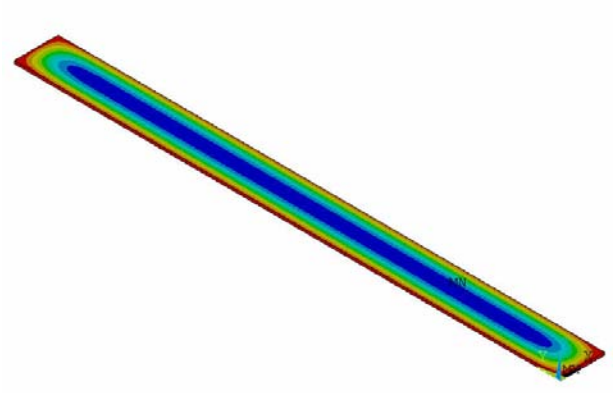
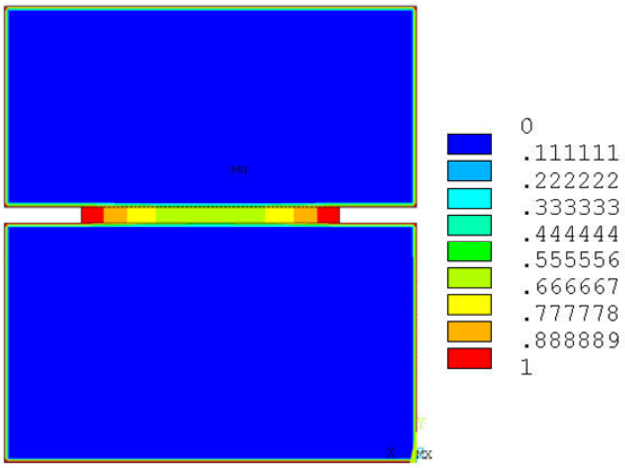


Figure 3.22: FEA model for moisture diffusion

The calculated results show that after 5 days of moisture soak, the underfill materials were fully saturated at the outside and about 60% saturated in the center as in Figure 3.23. G_c values of these samples after 5 days moisture soak at 85°C/85RH were found to be 5.2+/-1.2 J/m^2 as shown in Figure 3.24, dropped by ~40% compared to values under the un-soaked, room temperature condition.



(a)



(b)

Figure 3.23: Moisture diffusion results after 5 days moisture soak at 85^{o}C and 85RH (a) overview of underfill (b) cross section view

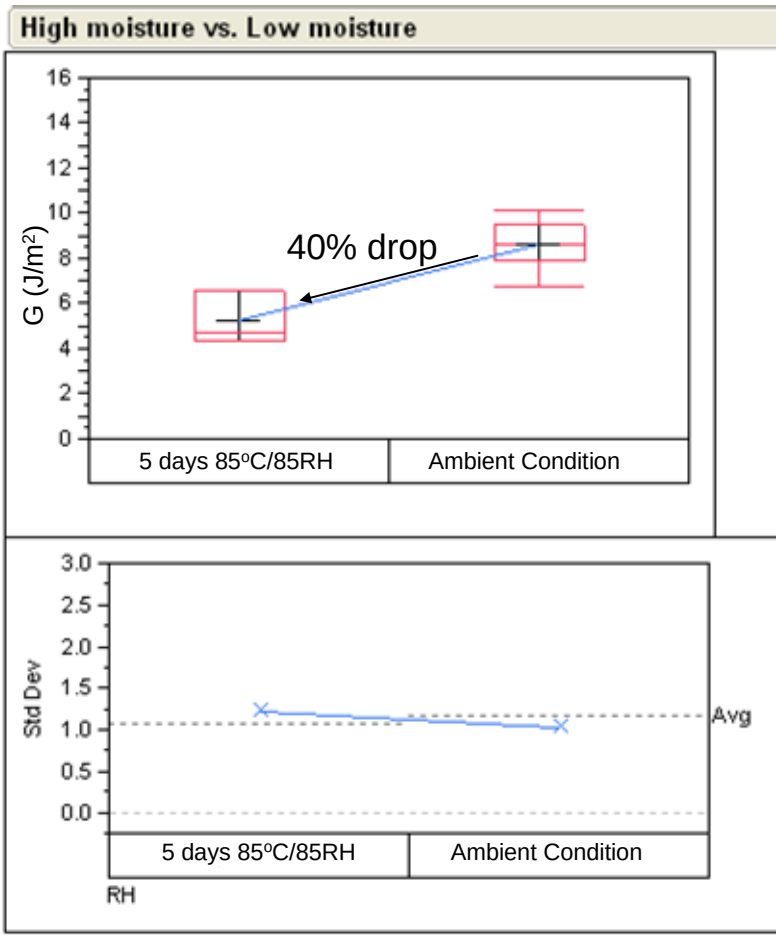


Figure 3.24: Moisture effect on the adhesion strength of Cu/underfill interface

The adhesion strength between solder resist film and underfill was also investigated in this study. Similar trends for the moisture effect were obtained in this interface as plotted in Figure 3.25. A decrease of 34% was found for samples soaked in the moisture chamber for 5 days compared to samples without moisture soak. These studies concluded that moisture concentration increase in underfill can significantly degrade the adhesion strength of Cu/UF and Cu/SR interfaces. Considering the energy release rates obtained from the model, Cu/SR interface is relatively more stable compared with Cu/UF interface for the given crack length.

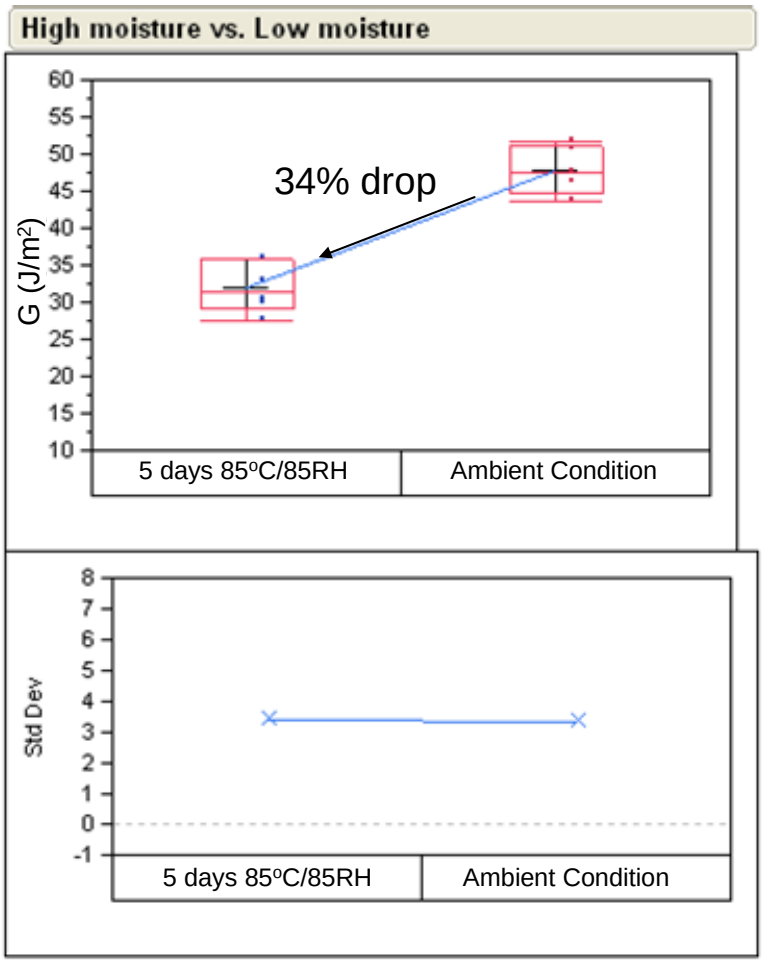


Figure 3.25: Moisture effect on the adhesion strength of Cu/SR interface

3.7 Conclusion and Discussion

In this chapter, we investigated the effect of underfill material properties on the reliability of flip-chip packages with fine-pitch Pb-free solder bumps and ultra low-k interconnects using high-resolution moiré interferometry technique and finite element analysis. Several failure modes were analyzed, including solder thermal fatigue, chip/underfill delamination, and delamination of low-k layers from the passivation. The effects of Tg, E, and CTE on ERR for various interfaces were separately investigated as a

function of underfill properties. The dominant parameters for each failure mode were identified and discussed. The key results are summarized as follows.

Solder fatigue: Simulation results reveal that the thermal cycling fatigue life of Pb-free solders depends heavily on the Tg and CTE of the underfill used, but is not very sensitive to the underfill modulus E. Underfills with high Tg and CTE close to that of solder bumps are preferred for longer fatigue lifetime.

Chip/underfill delamination: For this failure mode, Tg remains the key parameter in determining the delamination driving force. The ERR increased by a factor of about 5.5 times when Tg increased from 30^{o}C to 130^{o}C. The second important parameter is CTE, which caused a 100% increase in ERR when CTE increased from 20ppm/^{o}C to 40ppm/^{o}C. E also impacts the ERR even though the effect is not as large as Tg and CTE. A 67% increase was observed when the E increased from 5.4GPa to 10GPa.

Low-k dielectric/passivation delamination: Similar to the chip/underfill delamination, Tg plays the most important role for low-k delamination. The ERR value increased by 5 times when Tg of the underfill increased from 30^{o}C to 130^{o}C. E and CTE also have impacts on the ERR. An increase of 66% and 33% was found when E increased from 5.4GPa to 10GPa and CTE increased from 20ppm/^{o}C to 40ppm/^{o}C, respectively.

Contradictory requirements in underfill selection were found in this study. For example, underfill with high Tg is preferred for better solder fatigue life time, while underfill with low Tg is favored when considering low-k dielectric integrity. The requirements of underfill to provide good protection for both the solder joints and weak low-k dielectrics make underfill selection increasingly difficult. Proper selection of

underfill materials is required in order to achieve optimal reliability performance at both package level and chip level.

In the last section of this chapter, the adhesion strength of underfill to Cu and SR film under various moisture conditions was investigated. Moisture content in underfill was found to have significant impact on the interfacial adhesion strength. The adhesion energy was reduced by 40% and 34% respectively for Cu/underfill and Cu/SR interfaces after soaking the test samples in a moisture chamber at 85^{o}C/85RH for 5 days.

Chapter 4: Chip Package Interaction (CPI) and its Impact on Cu/low-k Interconnect Reliability

4.1 Introduction

In addition to reliability issues related to solder joints and underfill materials studied in chapter 3, mechanical failures in low-k interlayer dielectrics and related interfaces during flip-chip packaging processes have raised serious reliability concerns, especially when ultra low-k (ULK) materials are involved. This problem can be traced to interfacial fracture induced by CPI. During packaging processes, thermal stresses arise from the mismatch in the CTE's between the chip and the substrate, and can be directly coupled into the Cu/low-k interconnect structure to drive interfacial delamination. Thermal load on the package reaches a maximum during solder reflow before underfilling in the die (chip) attach process. The thermally induced shear and peeling stresses reach a maximum at the outermost corner bumps, driving interfacial crack formation and propagation in the Cu/low-k interconnect. Such reliability issues have generated extensive interests recently to investigate chip-package interaction and its impact on the reliability of flip-chip packages with Cu/low-k interconnects [1-8].

In this chapter, finite element method is used to study the CPI and its impact on the reliability of Cu/low-k interconnects. The thermo-mechanical behavior of flip-chip packages under CPI is first investigated. A three-dimensional (3D) multilevel sub-modeling method is developed to calculate the CPI induced crack driving force for interfacial delamination in Cu/low-k interconnect structures. The discussion was first focused on the effects of dielectric and packaging materials including different low-k

dielectrics and Pb-based and Pb-free solders. The discussion is then extended to structural optimization to improve the CPI reliability as the technology continues with dimensional scaling and implementation of porous ULK materials. Finally, results on CPI-induced crack propagation in the Cu/low-k interconnects are presented and the use of crack-stop structures to improve the reliability is discussed.

4.2. Modeling of Chip-Package Interactions

Finite element analysis is commonly used to evaluate the thermo-mechanical deformation and stress distributions in electronic packages. For stand-alone silicon chips, modeling results show that thermal stresses in Cu interconnect lines depend on the aspect ratio, i.e., the height to width ratio, and the degree of confinement from the surrounding dielectric materials, barriers, and cap layers (Figure 4.1) [9]. For a Cu line with an aspect ratio greater than 1, the stress state of the Cu line is triaxial. The Cu line behaves almost linear elastically under thermal cycling [10]. Wafer processing induced residual stresses in the interconnect structures have also been investigated using FEA [11]. The general behavior is in quantitative agreement with the results from x-ray diffraction measurements [10, 12].

After a silicon die is assembled into a flip-chip package, package deformation increases the thermo-mechanical stresses in the interconnect structures. Modeling the packaging effect on the thermo-mechanical stresses in the interconnect structure is challenging due to the large dimensional difference between the packaging and interconnect structures. To solve the problem, researchers from Motorola first introduced a multilevel sub-modeling technique to evaluate the ERR at interfaces in the interconnect structures after assembling a die into a flip-chip package [1, 2]. This technique bridges

the gap in the geometrical differences between the packaging level and the die level. The ERR's for various interconnect interfaces during packaging were calculated using 2D FEA models [1, 2].

In this study, a 3D FEA model was developed based on a 4-level sub-modeling technique to investigate the impact of CPI on Cu/low-k interconnect reliability, with a particular focus on the effects of low-k dielectric materials used to form the Cu/low k interconnect structures.

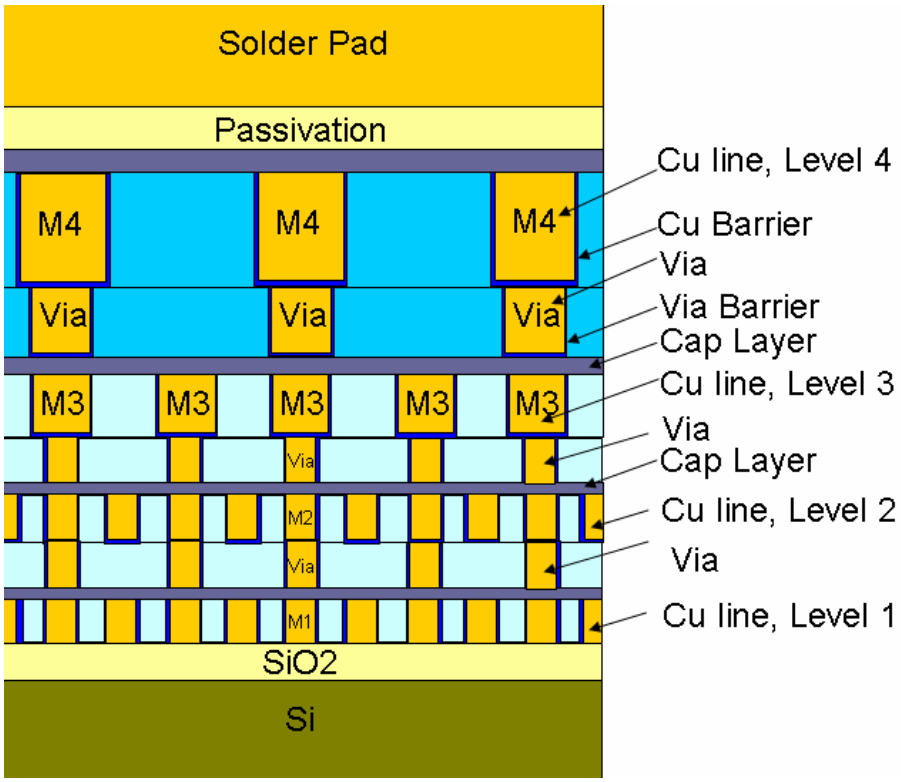


Figure 4.1: Cu/low-k structure schematics for FEA

4.2.1 Multilevel Sub-Modeling Technique

Level 1: Package level. It is used to investigate the thermal deformation of the whole flip-chip package. At this level, a quarter section of the package is modeled using the

symmetry condition as illustrated in Figure 4.2(a). No interconnect structure detail was considered because its thickness is too small compared to the whole package. Simulation results for this package level model were calibrated with experimental results obtained from Moiré interferometry.

Level 2: Critical solder level – A sub-model focusing on the critical solder bump region with much finer meshes as shown in Figure 4.2(b). From the simulation results for the package level modeling, the most critical solder bump is identified. The built-in cut boundary technique in ANSYS [13] is used for sub-modeling. At Level 2, a uniform ILD layer at the die surface is considered but still no detailed interconnect structure is included.

Level 3: Die-Solder interface level – A sub-model created based on Level 2 model using the cut boundary technique, as shown in Figure 4.2(c). Based on the Level 2 sub-modeling results, a large peeling stress is found at the die-solder interface. Level 3 model focuses on the die-solder interface region with the highest peeling stress (a small region of Level 2). It contains a portion of the die, the ILD layer and a portion of the solder bump. Still only a uniform ILD layer at the die surface is considered at this level and no detailed interconnect structure is included.

Level 4: Detailed interconnect level – A zoomed in sub-model further from Level 3, focusing on the die-solder interface region as shown in Figure 4.2(d). Here a detailed 3D interconnect structure is included. An interconnect structure with four metal levels and vias is considered, and the effects of multilevel stacks are discussed in Section 4.7.2. In this Level 4 sub-model, a crack with a fixed length is introduced along the center axis at several interfaces of interest. Energy release rate and mode mixity for each crack are

determined using a modified virtual crack closure technique which will be discussed in the next section.

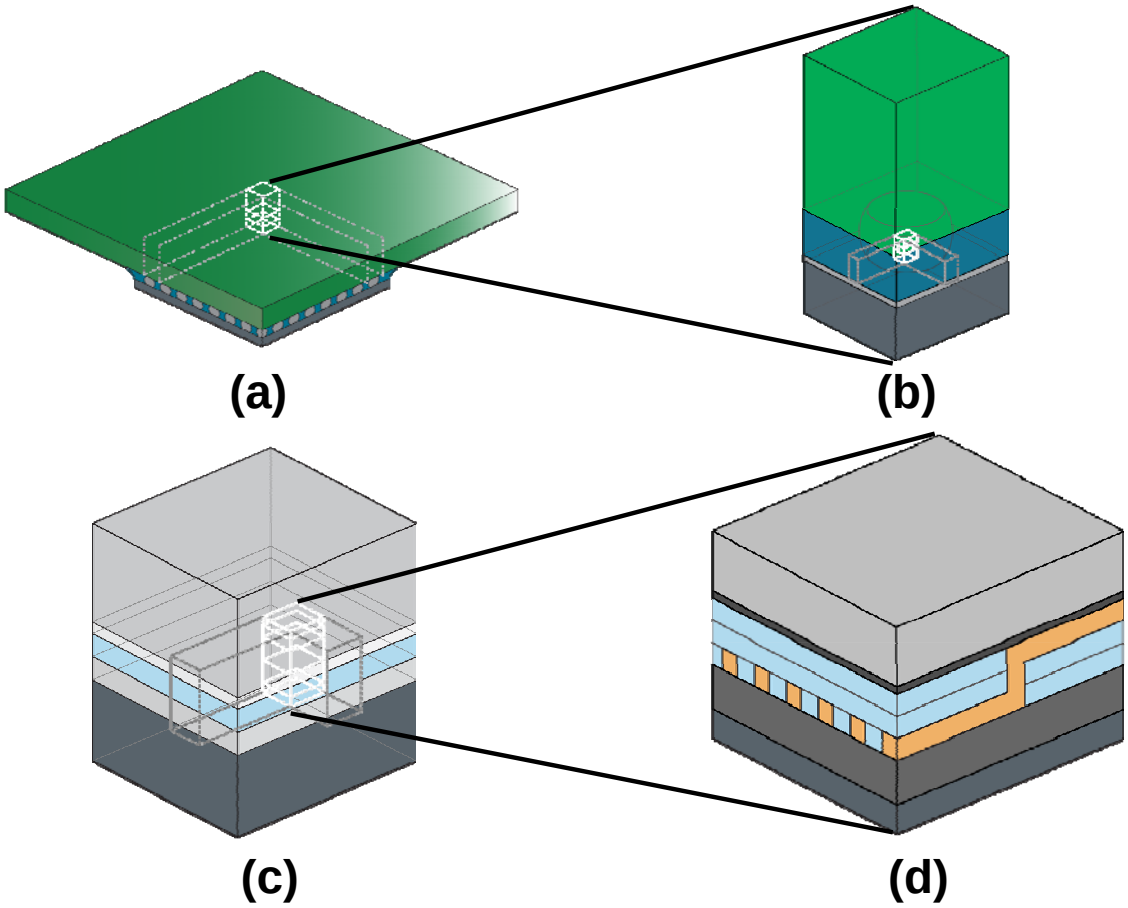


Figure 4.2: Illustration of four-level sub-modeling: (a) package level; (b) critical solder level; (c) die-solder interface level; (d) detailed interconnect level.

4.2.2 Modified virtual crack closure (MVCC) technique

To investigate the impact of CPI on the reliability of Cu/low-k interconnect and packaging structures, interfacial cracks are introduced in the models and the energy release rates as well as mode mixity are calculated as a measure of the crack driving force for interfacial delamination.

Several methods have been developed for calculating the interfacial fracture parameters within the framework of finite element analysis. The J-integral method has been widely used [14-16] and is a standard option in some commercially available FEA codes. This method is capable of calculating both the energy release rate and the mode mixity for 2D and 3D interfacial cracks, but it requires relatively fine meshes near the crack tip to achieve convergence and path independence of the numerical results.

A set of special finite element methods have also been developed to improve the numerical accuracy without requiring fine meshes, such as the singular element method [17], the extended finite element method (XFEM) [18], and an enriched finite element method [19, 20]. Implementation of these methods however is very involved numerically, which has limited its acceptance to problems with relatively simple geometry and material combinations.

Alternatively, Liu et al. [8, 21] calculated stress intensity factors by comparing the crack surface displacement with the analytical crack-tip solution, from which both the energy release rate and mode mixity were determined. This approach requires very fine meshes near the crack tip for the accuracy of the displacement calculation, and is not readily applicable for 3D problems.

With the material and geometrical complexities in the four-level modeling of CPI, a simple method using standard FEA codes along with relatively coarse meshes is desirable for the fracture analysis. A modified virtual crack closure (MVCC) technique [3, 22] has emerged to meet such a need, and is described as follows.

As illustrated in Figure 4.3, the MVCC method calculates the components of the energy release rate corresponding to the three basic fracture modes I, II and III,

separately. With the local stress/strain and displacement distributions obtained by the finite element modeling, both the energy release rate and the mode mixity for the interfacial cracks can be calculated accordingly. For the eight-node solid elements shown in Figure 4.3, the three energy release rate components G_I, G_{II} and G_{III} can be obtained as:

$$\begin{aligned} G_I &= \sum_i F_z^{(i_1)} \delta_z^{(i_2)} /(2\Delta A) \\ G_{II} &= \sum_i F_x^{(i_1)} \delta_x^{(i_2)} /(2\Delta A) \\ G_{III} &= \sum_i F_y^{(i_1)} \delta_y^{(i_2)} /(2\Delta A) \end{aligned} \qquad (4.1)$$

where $F_x^{(i_1)}$, $F_y^{(i_1)}$ and $F_z^{(i_1)}$ are nodal forces at node i_1 along the x, y and z directions, respectively, and $\delta_x^{(i_2)}$, $\delta_y^{(i_2)}$ and $\delta_z^{(i_2)}$ are relative displacements between node i_2 and node i_3 in the x, y and z directions, respectively. Note that, for simplicity, only one element set is shown along the crack front direction (y direction). The total energy release rate is then

$$G = G_I + G_{II} + G_{III} \qquad (4.2)$$

(4.3)

The criterion for interfacial delamination can thus be established by comparing the total energy release rate to the experimentally measured mode-dependent interface toughness, i.e., $G = \Gamma(\psi, \varphi)$.

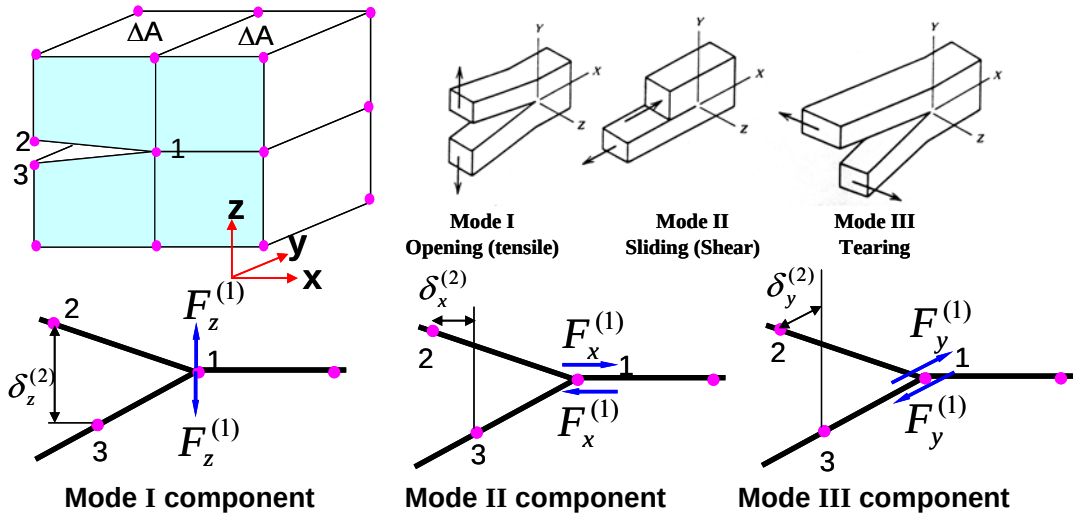


Figure 4.3: Schematic illustration of the modified virtual crack closure (MVCC) technique [9]

While the original virtual crack closure technique (VCCT) was proposed for cracks in homogeneous materials [23-25], it has been shown that care must be exercised in applying the technique for interfacial cracks [25-29]. As noted by Krueger [25], due to the oscillatory singularity at the interfacial crack tip, the calculated energy release rate and mode mixity might depend on the element size at the crack tip. It was suggested that the element size should be chosen small enough to assure a converged solution by the finite element model but also large enough to avoid oscillating results for the energy release rate. Furthermore, mode I and mode II in general could not be separated for interfacial cracks (except for cases with $\beta = 0$). The dividing up of the energy release rate components in Eq. 4.1 is therefore dependent on the element size, and so is that of the phase angles in Eq. 4.3. The total energy release rate on the other hand was found to be less sensitive to the element size [26, 27]. Several approaches have been suggested to extract consistent phase angles of mode mixity independent of the element size using the

VCCT [28, 29]. For simplicity, the phase angles defined in Eq. 4.3 are used in the subsequent discussion.

4.3 Package level deformation

The FEA results for the package level modeling can be verified using experimental results from Moiré interferometry. Since the thermal load used in the moiré measurement was from 102°C to 22°C, the same thermal load (102°C to 22°C) was applied in the modeling so as to directly compare the Moiré and FEA results. Figure 4.4 shows the z-displacement (package warpage) distribution along the die center line. The FEA and Moiré results are found to be in good agreement. Detailed Moiré results can be found in Reference 9.

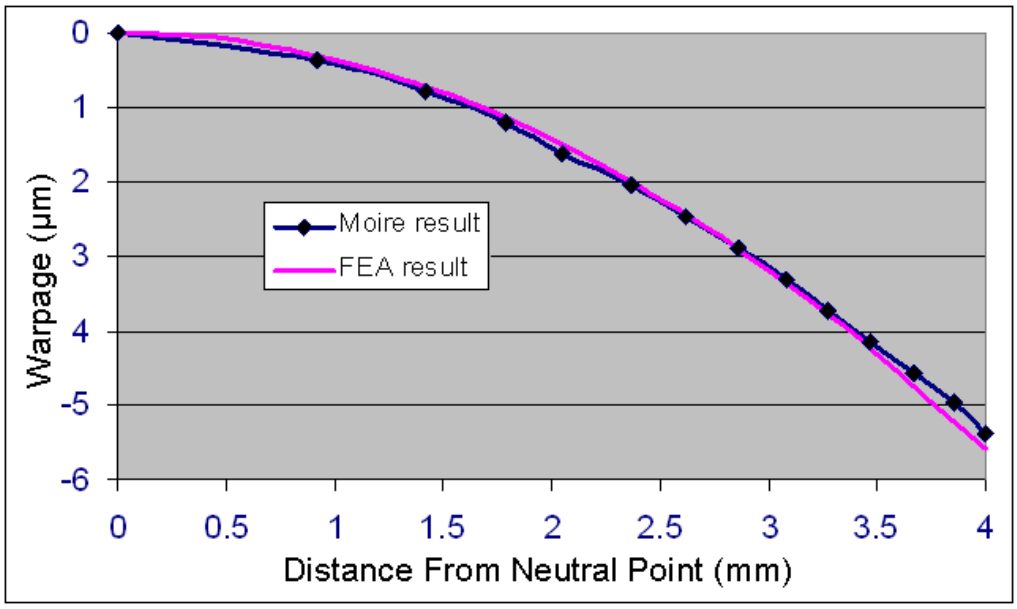


Figure 4.4: Comparison of FEA and moiré results of thermal deformation for the flip-chip package

4.4 Impact of CPI on different generation of low-k dielectrics

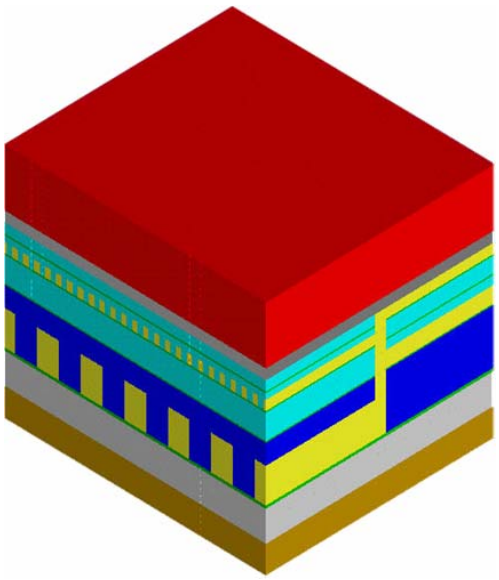
After verification with Moiré interferometry, the FEA model was applied to evaluate the energy release rates for low-k layer delamination in the interconnects during assembly. The material properties used in the modeling analysis are listed in Table 4.1. The mechanical behavior of all the materials in the structure was assumed to be linear elastic. Three low-k dielectrics were investigated, fully dense low-k OSG, porous low-k MSQ, and the latest porous ultra low-k material to represent the evolution history of low-k ILD's.

Ultra low-k dielectrics are desired in advanced technology nodes to improve the electrical performance. However, when porosity is introduced into the dielectric to reduce the dielectric constant, the mechanical properties deteriorate. The weak mechanical properties, e.g. low modulus and weak adhesion, raised a lot of reliability concerns during BEOL fabrication and packaging.

The purpose of this study is to understand the essence of the mechanical instability of ultra low-k dielectrics and find ways to optimize the package design and material selection to improve the reliability. The analysis was based on a 3D multilevel interconnect model with four metal levels, as shown in Figure 4.5. It was found that a 4-level 3D structure provided a realistic wiring structure to analyze the effect of porous low-k implementation in the interconnect structure. In this structure, the pitch and line dimensions in the first two metal layers (M1 and M2) were doubled in the third layer (M3), and were doubled again in the fourth layer (M4), approximately simulating the dimensional hierarchy in real interconnect structures.

Table 4.1: Mechanical properties of interconnect materials [7, 9]

Materials	**E (GPa)**	**ν**	**α (ppm/°C)**
Si	162.7	0.28	2.6
Cu	122	0.35	17
SiO_2	70	0.34	0.5
OSG (k~3.0)	17	0.3	8
MSQ (k~2.7)	10	0.3	10
ULK (k~2.4)	4	0.3	18



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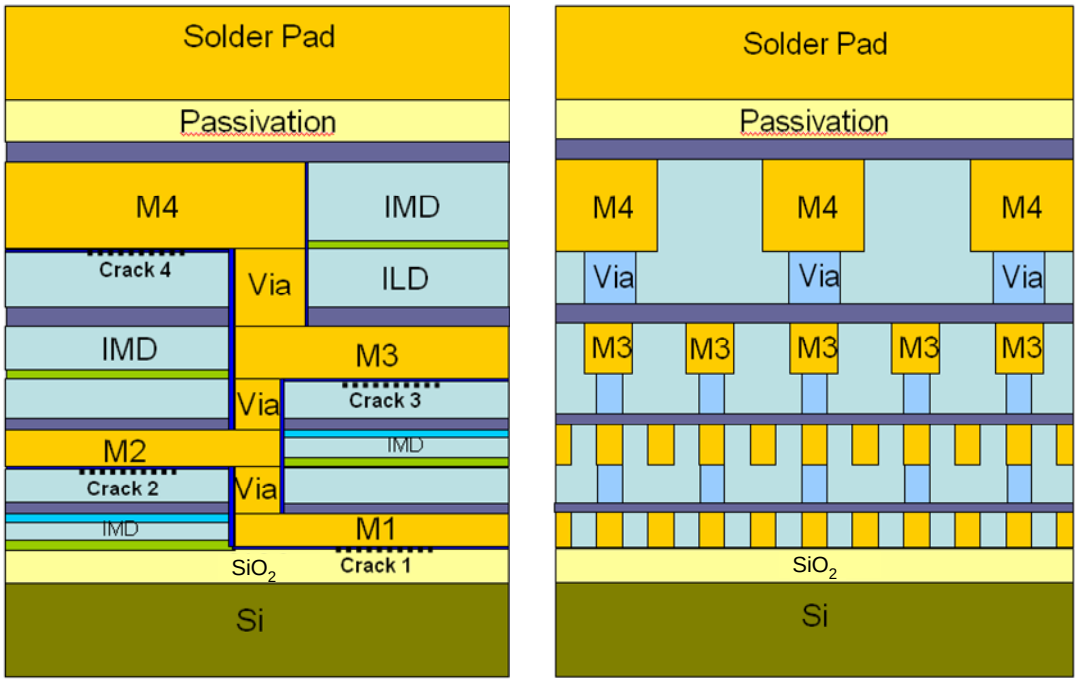


(b) (c)

Figure 4.5: FEA model of 3D 4-layer interconnect

(a) 3D view (b) Cross-sectional view (c) Side view

To calculate the energy release rate for ultra low-k layer delamination, defects were introduced at several relevant interfaces as shown in Figure 4.5. Each crack had a width of 0.1 μm and a length of 2 μm extending in the multiple wiring directions. Results of the ERRs of the interfacial cracks in the four-level interconnect models with three different low-k dielectrics are summarized in Figure 4.6. The calculated ERRs increase dramatically from OSG to MSQ and are the highest for ultra low-k, especially for crack 3 which is the low-k dielectric interface closest to the solder pad and has the largest delamination driving force among all four cracks. Among the dielectric materials, the ERR was the lowest for OSG, which had the highest E. For the ultra low-k material which

had the lowest E, the ERR value for crack 3 was about 6 times as high as that of OSG, indicating that the on-chip interconnect fabricated with ultra low-k dielectrics would need about 6 times higher adhesion strength at the interface of crack 3 in order to maintain a mechanical reliability equivalent to interconnects fabricated using OSG dielectrics.

Since ultra low-k materials are desired for 45nm technology and beyond according to the ITRS roadmap [30], this result indicated that CPI represents a major concern to interconnect reliability due to the weak mechanical properties of the components and the interfaces.

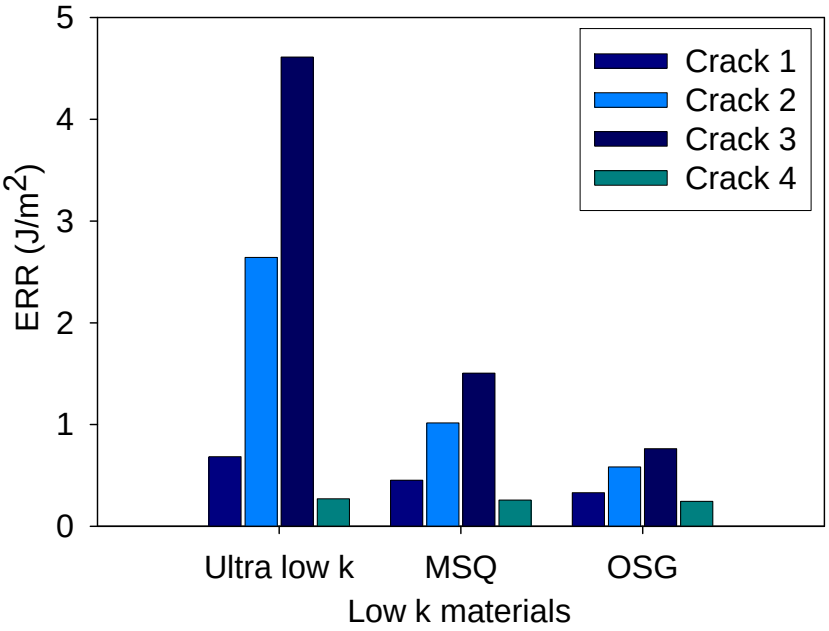


Figure 4.6: Comparison of CPI-induced energy release rates in the four-level interconnects with low-k and ultra low-k ILDs.

4.5 Effect of solder materials on CPI

The processing step causing the highest thermal load in flip-chip package assembly is the die attach step before underfilling. The solder reflow occurs at a temperature higher than the solder melting point and afterwards the package structure is cooled down to room temperature. Without the underfill serving as a stress buffer, the thermal mismatch between the die and the substrate can generate a large thermal stress at the solder/die interface near the die corner, creating condition for driving interfacial delamination. As the semiconductor industry shifts from Pb-based solders to Pb-free solders, the effects of solder material properties on CPI reliability become a concern.

In this section, the effect of CPI on the reliability of Cu/ULK interconnects was studied for the eutectic and lead-free solders with different reflow cycles: 220^{o}C to 25^{o}C for eutectic solder and 260^{o}C to 25^{o}C for lead-free solder, respectively. The material properties used in these calculations are shown in Table 4.2. The substrate in the package was organic and with a die size of 8mm by 8mm. Results are summarized in Figure 4.7. The eutectic solder package had a lower crack driving force for interfacial delamination due to its low reflow temperature and more compliant solder properties. In contrast, the driving force for the lead-free solder package was more critical due to the high reflow temperature and the high Young's modulus of the lead-free solder material, indicating that the implementation of lead free solder for flip-chip packages would pose higher threats to the mechanical reliability of ultra low-k interconnects. Therefore structural optimization is essential to maintain the mechanical stability during assembly which will be discussed in the following sections.

Table 4.2 Materials properties for high-lead, eutectic lead, and lead-free solders; [9]

(The modulus values are a function of temperature, T)

Solder Material	E (GPa)	ν	α (ppm/°C)
Eutectic	75.84-0.152*T	0.35	24.5
Lead-free	88.53-0.142*T	0.40	21.5
Underfill	6.23	0.40	40.6
Organic substrate	Anisotropic elastic [9]		16 (in plane) 84 (out of plane)

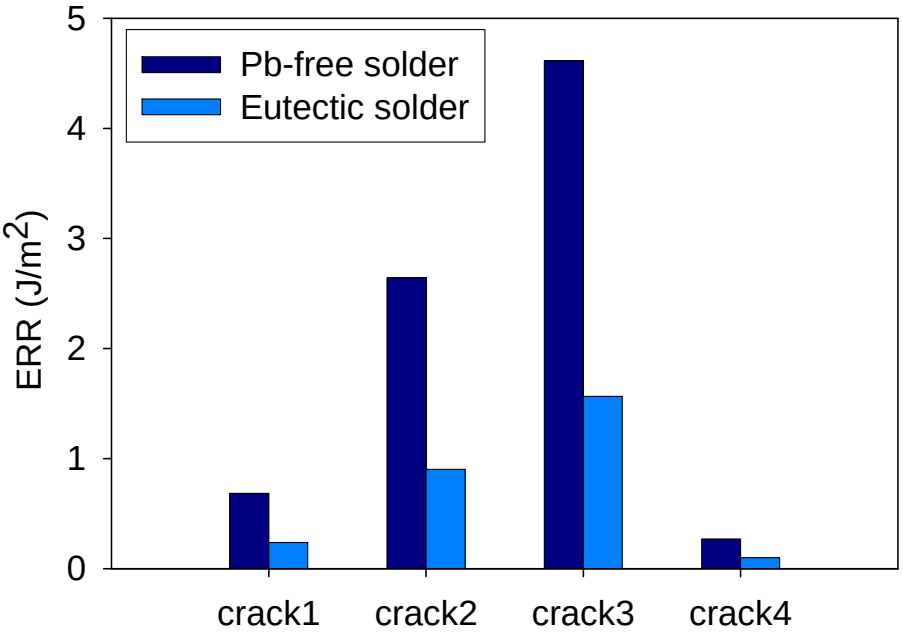


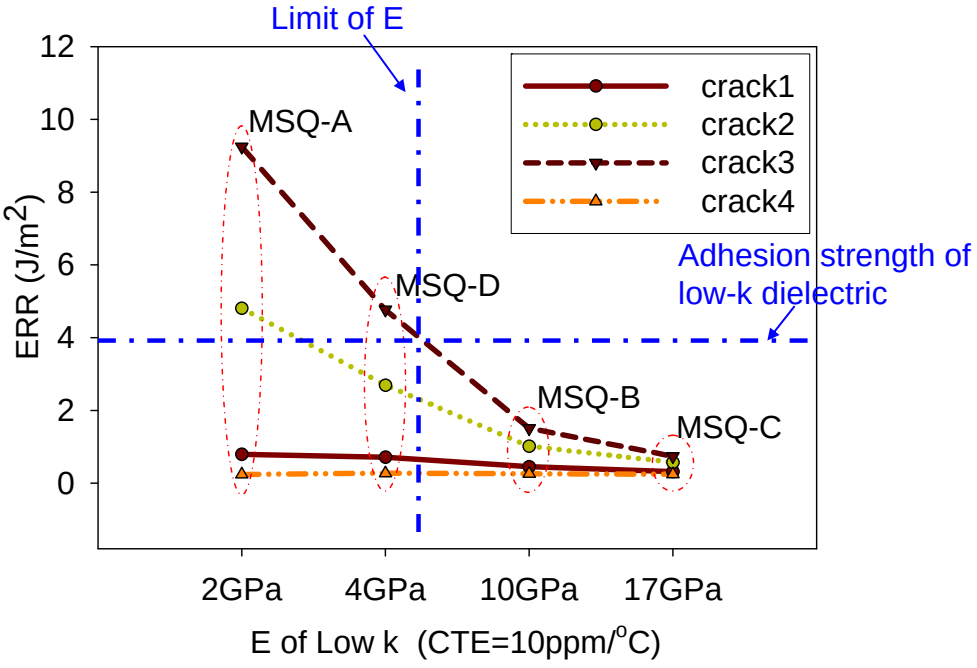
Figure 4.7: Effect of solder materials on ERR in the interconnects

4.6 Effect of low-k material properties on CPI

As mentioned in section 1.3, weak mechanical properties of porous low-k materials have raised many reliability concerns in the Cu/low-k interconnects during fabrication and assembly. Various porous low-k dielectric materials are being developed to achieve better reliability performance without sacrificing the RC delay. To understand the effect of dielectric material properties on low-k interconnect stability, the CPI-induced delamination driving force was compared for several porous MSQ materials (A to G) with different thermo-mechanical properties as listed in Table 4.3. Some of the MSQ materials are artificial and used only for the purpose of separating the effect of E and CTE on low-k dielectric delamination which can't be achieved by comparing real MSQ materials. The results are plotted in Figure 4.8(a), which shows a good correlation between ERR and E. Comparing porous MSQ-A (k ~ 2.3) with dense MSQ-C (k ~ 3.0), with similar CTE, their ERR values were quite different due to the variation in E. The likelihood of low-k delamination under CPI increased rapidly as the E of low-k dielectrics was reduced. Interestingly, for the porous MSQ-D to MSQ-F, even though they had a very different CTE, their ERR values were about the same as shown in Figure 4.8(b). There appeared to be little effect of CTE. In contrast, the ERR increased considerably with decreasing E. Therefore, for low-k dielectrics, E was the dominant property with regard to mechanical reliability. The fracture toughness of ultra low-k dielectrics is usually below 4 J/m^2 for mode I delamination [9]. In order to maintain low-k integrity under CPI, the crack driving force has to be below 4 J/m^2, which corresponds to an E values greater than 5 GPa as shown in Figure 4.8(a).

Table 4.3: Material properties of MSQ

Materials	E (GPa)	ν	α (ppm/°C)
MSQ-A	2	0.35	10
MSQ-B	10	0.3	10
MSQ-C	17	0.3	10
MSQ-D	4	0.3	10
MSQ-E	4	0.3	4
MSQ-F	4	0.3	18
MSQ-G	4	0.3	26



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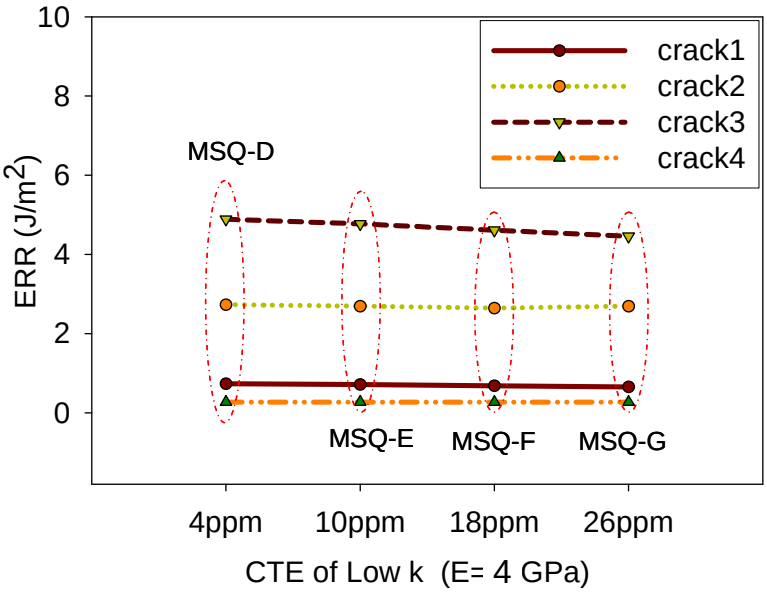


(b)

Figure 4.8: Effect of low-k material properties on ERR (a) E (b) CTE

4.7. Structural optimization to reduce the risk of low-k dielectric delamination

The scaling of interconnect structures has led to highly complex architectures with over 10 metal layers, sub-50 nm dimensions, and ultra low-k dielectrics. Dimensional scaling and the implementation of ultra low-k dielectric have raised serious concerns on chip-package interaction and low-k interconnect reliability. Structural optimization in both the package level and interconnect level are required to sustain the mechanical reliability caused by implementation of weak ultra low-k dielectrics.

4.7.1 Package level structural optimization

According to the Moiré experiment and FEA results, the Cu/low-k interconnect directly on top of the corner bump had the highest interfacial peeling and shear stresses and it was the most prone to fracture during packaging or subsequent stressing tests.

Therefore, this region is of great interest for investigation. Figure 4.9 shows a 2D 2-level FEA model that was used in this study to simulate the Pb-free solder reflow process. Detailed UBM and solder pad structure are taken into account in the solder model as shown in the schematic. For simplification, the multi-layer Cu/low-k interconnect was simulated as a uniform low-k layer with an effective material properties that was deduced based on the Cu density in the interconnect structure. Therefore, the quantitative value of stress in low-k layer can be considered as an average stress and used as an indicator of the stability of low-k dieletrics. This much detail is sufficient to investigate the geometric effect and structural optimization at package level.

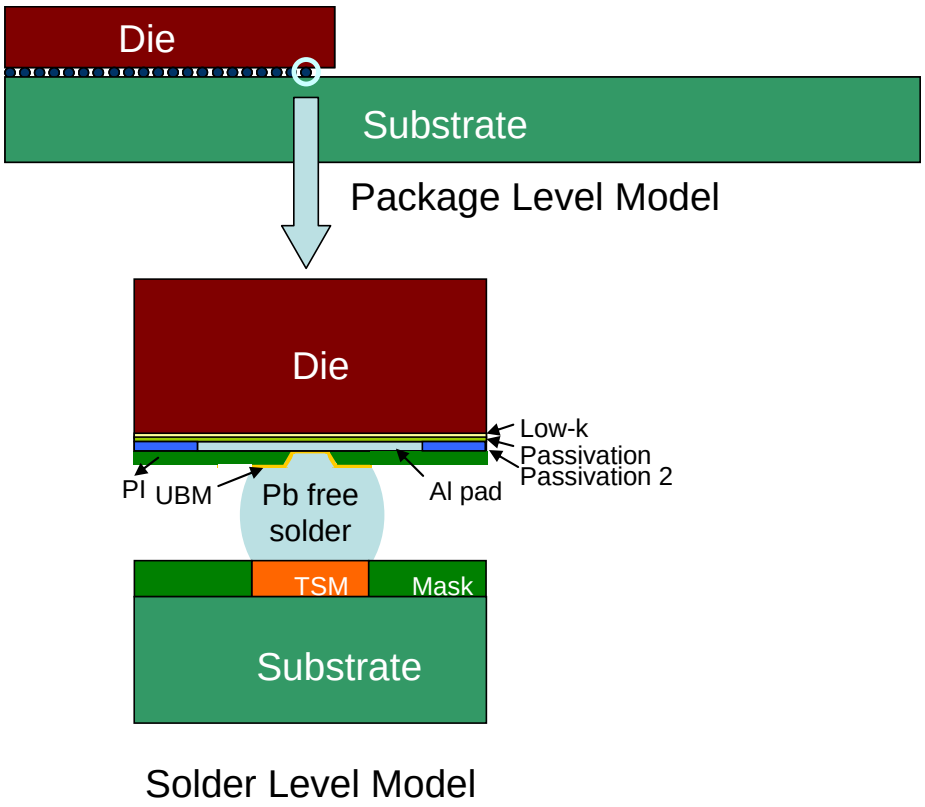
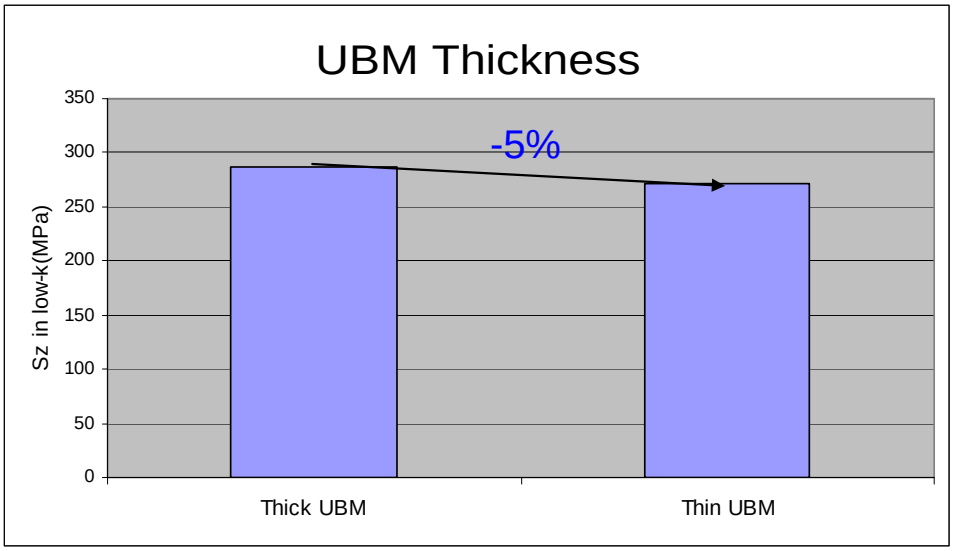


Figure 4.9: FEA model for the study of package level structural optimization

The thermal stresses induced by packaging are transferred into low-k interconnects via the Cu UBM, Al solder pad, and passivation layers. These layers act as a stress buffer between solder bump and low-k interconnect. The amount of stress transferred into the low-k material and the corresponding strain can be reduced by optimizing the structural design. Several geometric factors like UBM diameter, UBM thickness, Al pad thickness, and passivation thickness were investigated in this study. The results are summarized as the following.

I. Effect of UBM design:

Cu UBM thickness and diameter were first studied. The maximum thermal stress along the vertical direction Sz was calculated for UBM with different thicknesses and diameters. Figure 4.10(a) shows a comparison between thick UBM and thin UBM structures. A slight decrease, ~5%, in the stress of the low-k material was observed by reducing the UBM thickness by ~50%. In contrast, shrinking the UBM diameter is more effective in reducing the low-k thermal stress as demonstrated in Figure 4.10(b). A 17% reduction in the stress can be achieved by shrinking the UBM diameter by only 20%. Therefore, using a UBM structure with smaller diameter is beneficial to the low-k mechanical stability under CPI.



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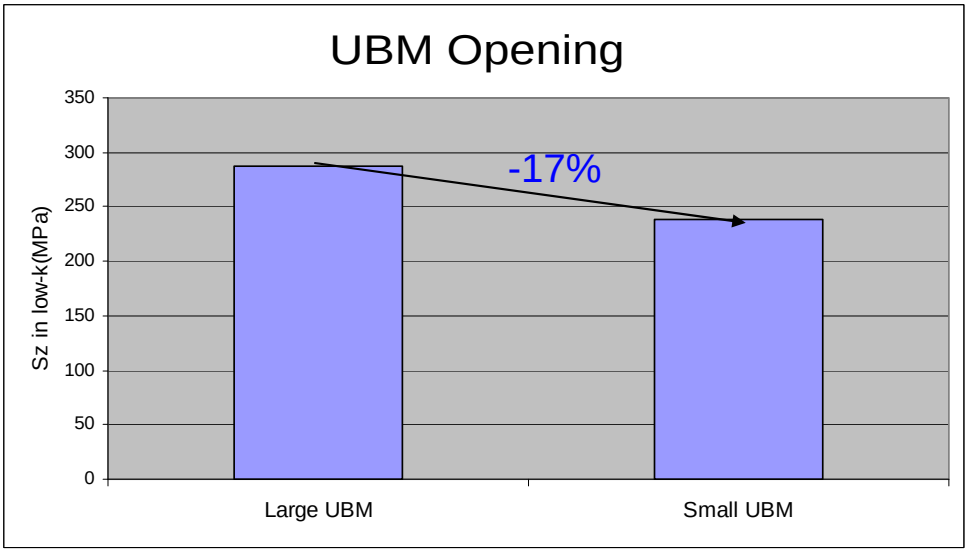
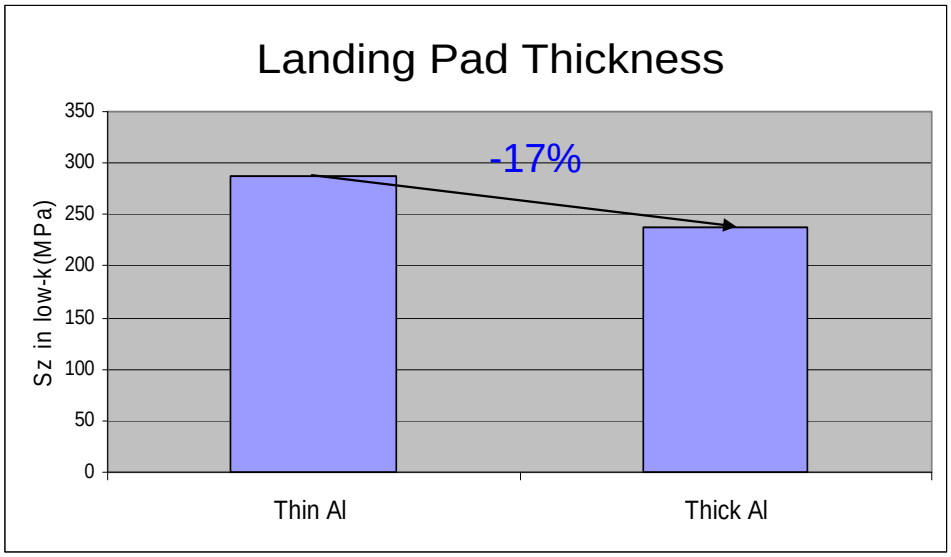


(b)

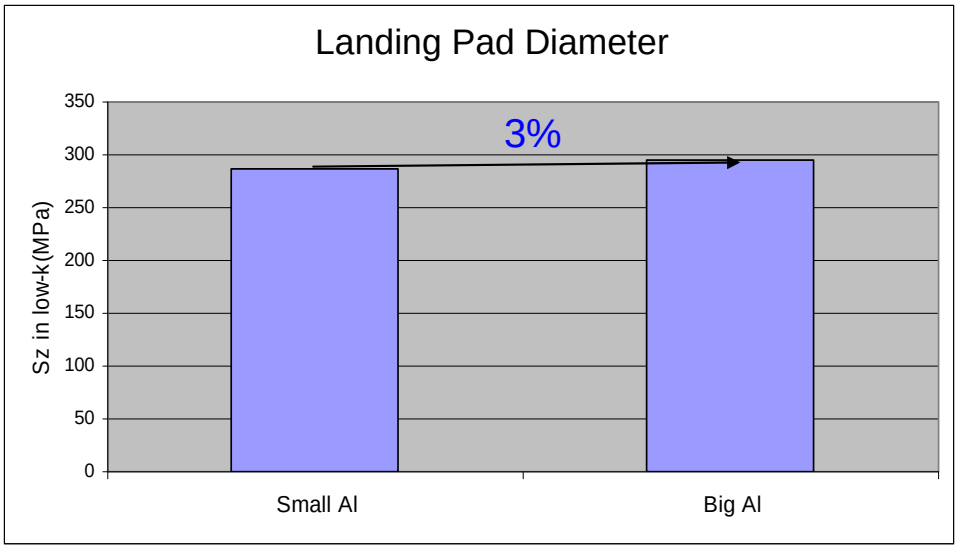
Figure 4.10: Effect of UBM geometry on vertical stress in low-k layer (a) UBM thickness (b) UBM opening

II. Effect of Al pad structure:

The effect of Al pad structural design was also investigated. Similar to the UBM study, comparisons between Al pad structures with different thicknesses and pad diameters were made as shown in Figure 4.11. The thickness of Al pad turns out to have a greater impact on the thermal stress level in low-k than the diameter of the pad. A decease of 17% in the low-k stress was obtained for a ~80% thickness increase in the pad as shown in Figure 4.11(a), while the stress remains constant as the diameter of Al pad was increased from 90μm to 120μm as in Figure 4.11(b).



(a)



(b)

Figure 4.11: Effect of Al pad geometry (a) Landing pad thickness (b) Landing pad diameter

III Effect of passivation thickness:

The passivation layer is another important stress buffer layer for low-k dielectrics. Increasing its thickness can also alleviate the stress level in low-k dielectrics. Figure 4.12 demonstrated a decrease of 10% in the stress as the passivation thickness was increased from 0.8 μm to 2.3 μm.

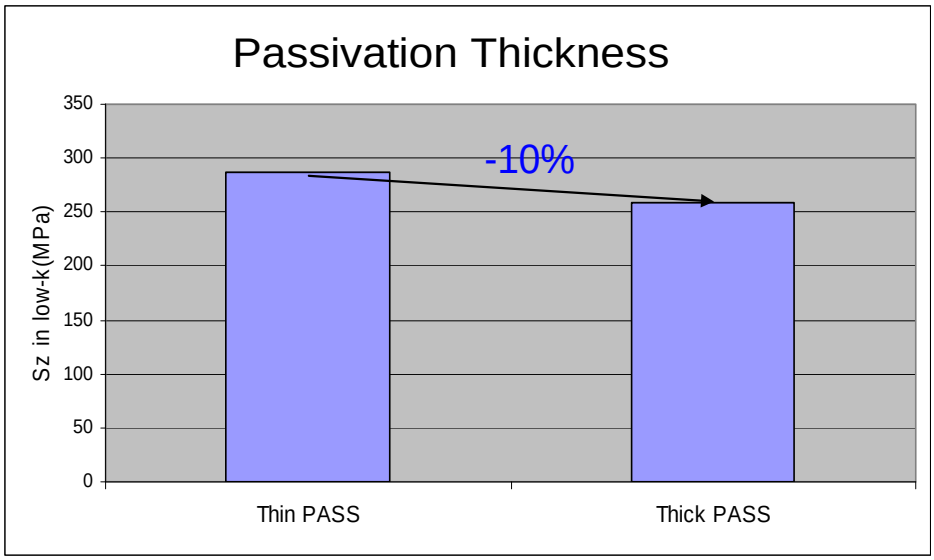


Figure 4.12: Effect of passivation layer thickness

In summary, the thermal stress of low-k dielectrics can be reduced by increasing the thickness of the buffer layers between the solder and low-k layer including UBM, Al pad, and passivation. Shrinking the UBM diameter can reduce the stresses transferred into low-k materials as well. Structural optimization in the Cu UBM, Al pad, and passivation layer is quite effective in maintaining the mechanical stability of Cu/low-k interconnects during assembly and also very important when ultra low-k with weak mechanical properties and Pb-free solder bumps are incorporated into the package for advanced technology nodes.

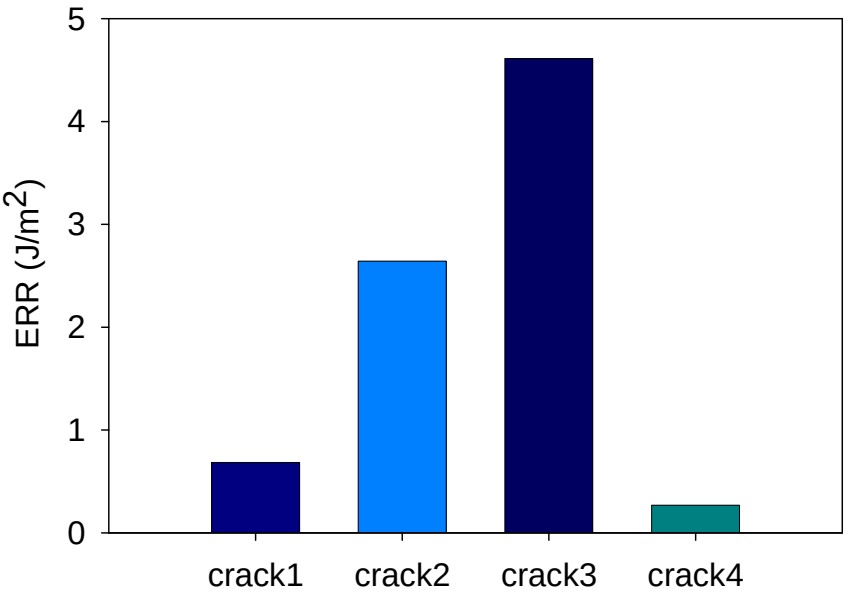
Besides these geometric factors, there are other techniques to mitigate the impact of CPI on the reliability of low-k interconnect during assembly. One of these techniques is called pad shift design in which the thermal mismatch between die and organic substrate is compensated by adjusting the metal pads on the substrate [31]. Another technique that is widely adopted is the redistribution layer (RDL) technique [31]. The

idea of this method is to avoid placing the weak low-k dielectrics directly on top of solder bump, especially on those corner bumps with large stress concentration during reflow. A metal trace called a redistribution line therefore is used to electrically connect the solder and low-k interconnects without direct contact right at the peripheral pads. Significant reliability improvement for low-k dielectrics can be achieved by using the RDL [31].

4.7.2 Interconnect level structural optimization

This section is focused on low-k layout optimization to improve reliability. The study reported here is based on a similar multilevel interconnect model as in section 4.4. It is of interest to find out whether different combinations of low-k and ultralow-k dielectrics in selective metal layers could improve mechanical reliability. Energy release rates were calculated for horizontal cracks placed at each metal level at the interface as shown in Figure 4.5. Results of the ERRs of the interfacial delamination in the four-level interconnect model were summarized in Figure 4.13 for three different ILD combinations. The first model (Figure 4.13(a)) used ultra low-k materials in all layers except metal 4 in which SiO_2 was used. In this case, the interfacial crack at the level 3 (crack 3) had the largest ERR. This is to be expected since the level 3 is the ultra low-k interface closest to the solder bump. In the second model (Figure 4.13(b)), a fully dense low-k OSG was used at level 3, which is mechanically stronger than ULK. Consequently, the ERR of crack 3 was reduced and the effect of elastic mismatch shifted the largest ERR to crack 2 in the M2 level and the magnitude of ERR was reduced compared to that of crack 3 in Model 2. In model 3 (Figure 4.13(c)), hybrid structure, OSG/ULK, was used at level 3, replacing OSG from the previous model. It was found that the ERRs for crack 2 dropped by a small amount while ERR for crack 3 increased slightly, indicating

ULK/dense low-k hybrid structure can achieve better reliability performance than a full low k structure. A comparison of these three cases was given in Figure 4.13(d). The results indicated that the multilevel stacking structure can be optimized to minimize the CPI effect on ULK interconnect reliability.



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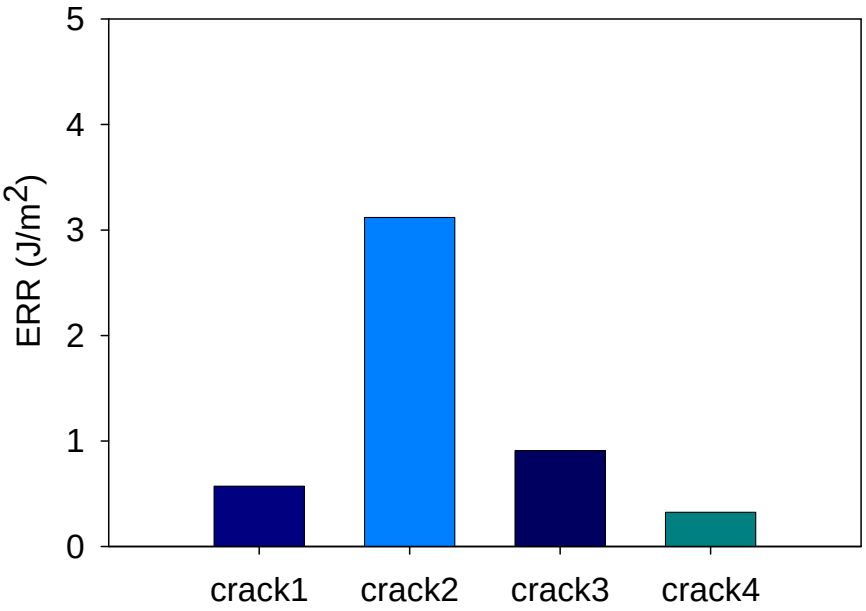
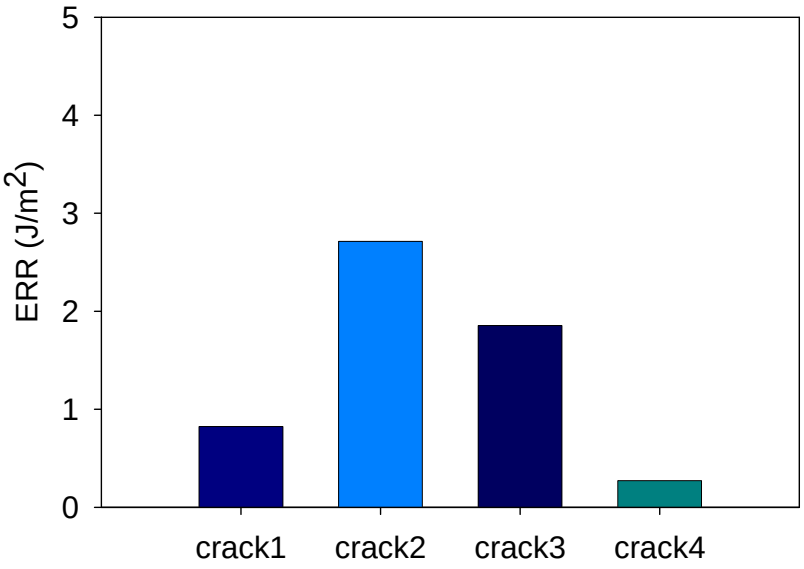

5
4
3
2
1
0
ERR (J/m2)
crack1
crack2
crack3
crack4

(b)


5
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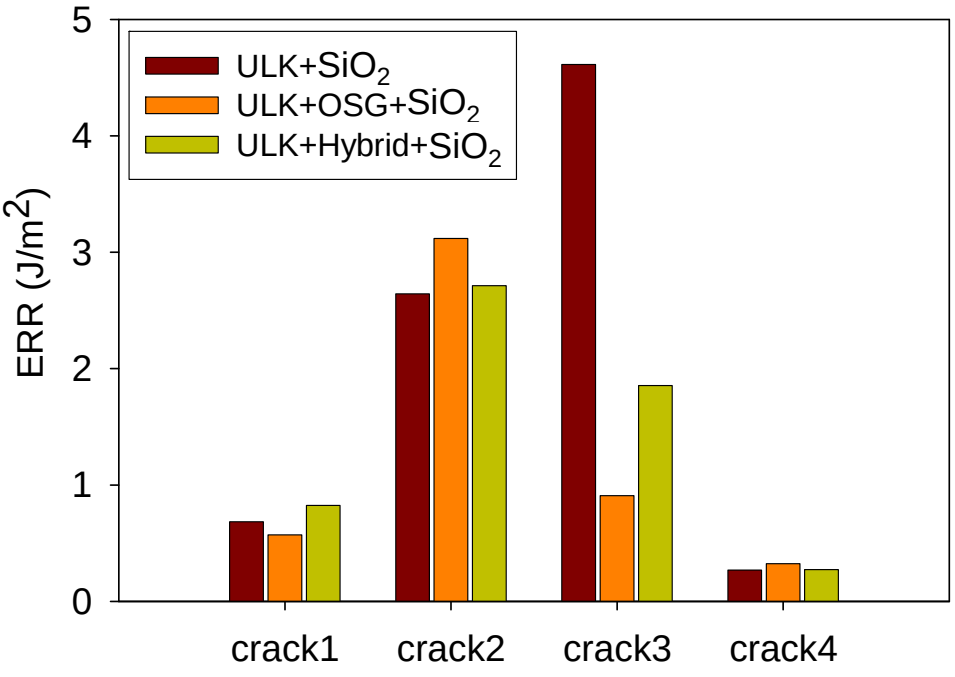
ERR (J/m2)
crack1
crack2
crack3
crack4

(c)



(d)

Figure 4.13: Effect of interconnect layout on ERR (a) low-k/SiO_2 (b) low-k/OSG/SiO_2 (c) low-k/hybrid/SiO_2 (d) comparison of the three cases

4.8 Crack propagation in low-k interconnects and crack stop design

In previous section, the energy release rate for low-k delamination in the interconnect was investigated for static cracks. In this section, the study was extended to the dynamic crack propagation in the low-k interconnects and the crack stop structure design to protect Si dies.

Firstly, the crack propagation path in a 6-layer Cu/low-k interconnects was predicted by use of finite element method. And then local crack stops were added into the model and their effect on crack propagation was studied. Finally, the fracture toughness

of crack stops used to prevent crack from propagating was measured by experiments. The effect of crack stop structures and their design rules for 45nm technology and beyond were discussed.

As a crack propagates in a multilevel interconnect structure, both the energy release rate and the mode mixity at the crack tip vary. In reality, the crack does not always propagate along one interface. Depending on the local material combination and geometry, an interfacial crack can kink out of the interface, causing cohesive fracture of the low-k materials. Similarly, a cohesive crack may deflect into a weak interface. The crack propagation path depends on the loading conditions as well as material properties (including interfaces) and geometrical features in the interconnect structure. A general rule of crack propagation, as suggested by Hutchinson and Suo [32] for anisotropic materials and composites, may be stated as follows: a crack propagates along a path that maximizes G/Γ, the ratio between the energy release rate and the fracture toughness. While cohesive fracture in an isotropic material typically follows a path of mode I ($\psi = 0$), the mode mixity along an interfacial path varies and so does the interfacial fracture toughness. Therefore, the crack propagation not only seeks a path with the largest energy release rate, but also favors a path with the lowest fracture toughness, either interfacial or cohesive.

Due to the complexity in the materials and structures, modeling of crack propagation in multilevel interconnects has not been well developed. Experiments have shown that cracks often propagate from the global-level interconnects to local levels that

are close to devices, eventually causing die cracking. Figure 4.14 depicts a FEA model to study the crack propagation induced by CPI in a multilevel interconnect.

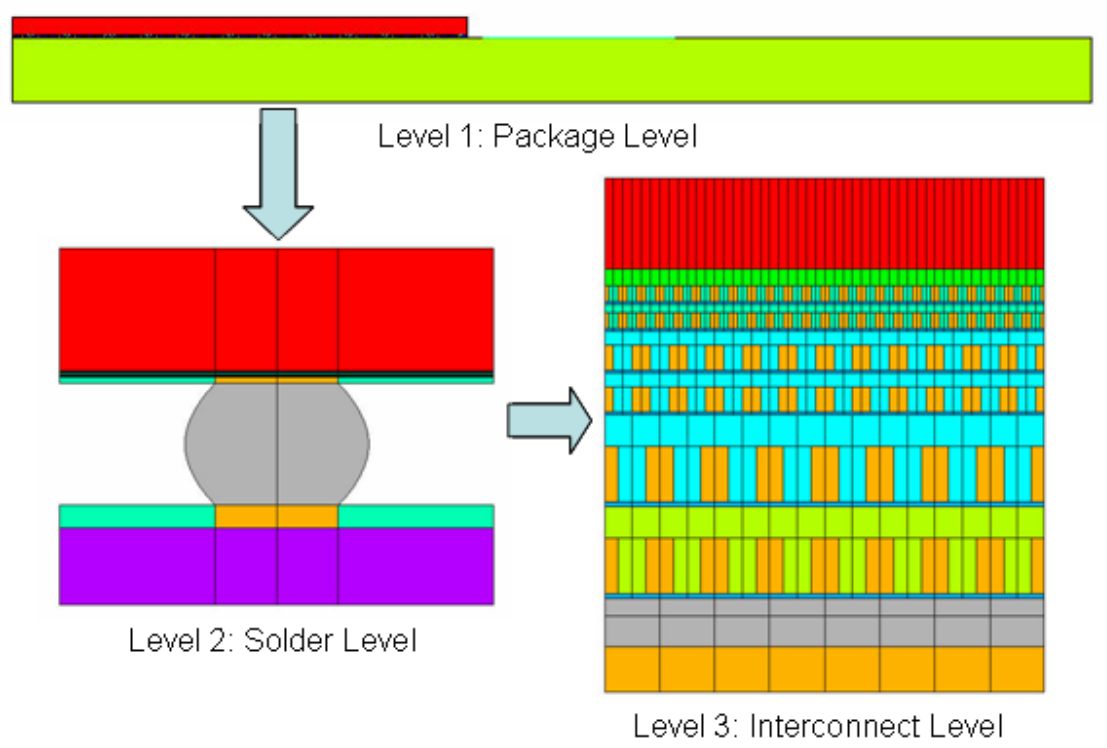


Figure 4.14: Three sub-level interconnect model for crack propagation studies

Similar to the description in section 4.2.1, this FEA model utilizes 3 sub-level models. Level 1 is the package level for investigating the overall thermal deformation for the flip-chip package. Simulation results for this package level were verified with experimental results obtained from Moiré interferometry. Level 2 is a sub-model with much finer meshes and focus on the critical solder bump region at the outermost chip corner. Level 3 contains detailed features for the interconnect structure with six metal levels. In this structure, the pitch and line dimensions in the first two metal levels (M1 and M2) are doubled in the third level (M3) while the fourth level (M4) is 1.5 times the

dimension of M3. The crack tip opening displacement method (CTOD) and the maximum hoop stress criterion were employed to study the crack propagation behavior. [32-34]

An example of crack propagation in a real interconnect structure due to CPI was already shown in Figure 4.15 [35]. The crack propagated from the upper levels to the lower levels, eventually causing failure by die cracking [36]. In this 2D multi-level FEA model the crack was assumed to initiate at the global-level interface, where a higher energy release rate was shown to exist than at local-level interfaces.

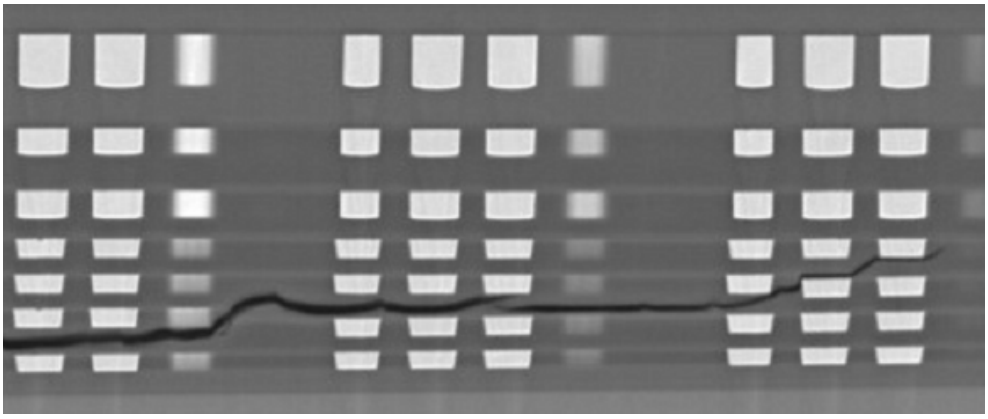
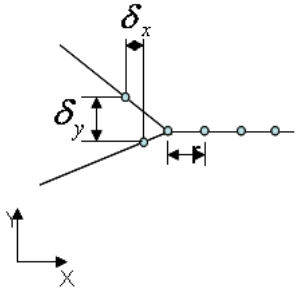


Fig. 4.15: Crack propagation in a multilevel interconnect

The CTOD method was employed to calculate the mode mixity at each crack tip by stress intensity factor K as the crack extended (Figure4.16) and then the maximum hoop stress criteria was used to predict the crack propagation direction as shown in Eq. (4.4).



$$K_1 = [A\cos(\varepsilon \ln r) + B\sin(\varepsilon \ln r)]/D$$
$$K_2 = [-A\sin(\varepsilon \ln r) + B\cos(\varepsilon \ln r)]/D$$
$$A = \delta_y - 2\varepsilon\delta_x \quad B = \delta_x + 2\varepsilon\delta_y \quad D = \frac{8}{E^* \cosh(\pi\varepsilon)}\left(\frac{r}{2\pi}\right)^{1/2}$$
$$G = \frac{1}{E^* \cosh^2(\pi\varepsilon)}\left(K_1^2 + K_2^2\right)$$

Figure 4.16: Crack Tip Opening Displacement Method (CTOD)

$$\sigma_{\theta\theta}(r,\theta) = \frac{\mathrm{Re}\left[Kr^{i\varepsilon}\right]}{\sqrt{2\pi r}}\cos^3(\frac{\theta}{2}) - \frac{\mathrm{Im}\left[Kr^{i\varepsilon}\right]}{\sqrt{2\pi r}}3\cos^2(\frac{\theta}{2})\sin(\frac{\theta}{2})$$
$$\tan(\frac{\theta^*}{2}) = \frac{2\tan\psi}{1+\sqrt{1+8\tan^2\psi}} \qquad (4.4)$$

The crack propagation path obtained by simulations is plotted in Figure 4.17, propagating from the upper levels to the lower levels. The actual path may not be exactly as shown since it can be affected by process defects and material inhomogeneity in the low-k interconnects. Nevertheless, the overall crack behavior can still be deduced from the simulation. The result also demonstrated that, as the crack propagated toward the local levels and the total crack length increased, the energy release rate continued to increase, indicating an unstable crack growth.

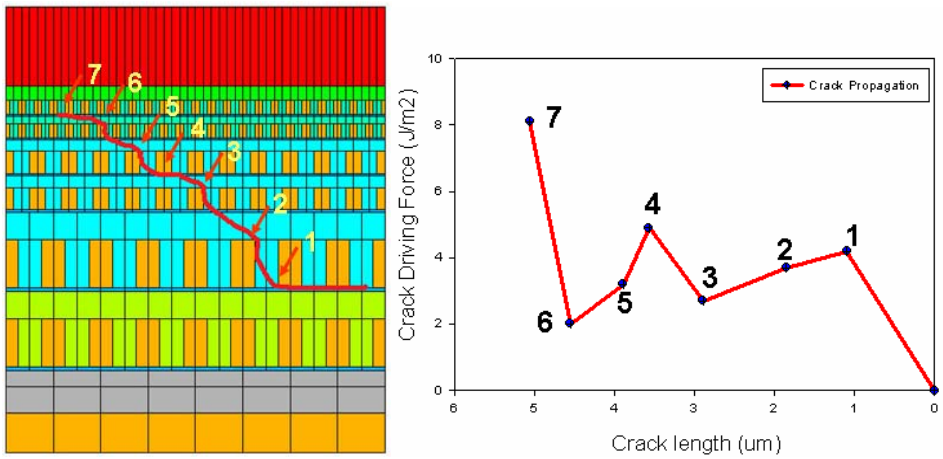


Figure 4.17: ERR for crack propagation

A major challenge in packaging Si die is to prevent cracks propagating from the die edge to the active area of a chip. One way the industry has been practicing to suppress crack propagation is to implement crack stop structures into the interconnect. The effect of crack stop structures was analyzed in this section. Dummy Cu crack stops at via levels were added into Cu/low-k interconnect as local reinforcements. The simulation result showed that the crack driving force was suppressed by the crack stop structure as shown in Figure 4.18. Meanwhile, the experiments revealed that the toughness of interconnects was increased due to the implementation of the crack stop structure, thus demonstrating its effectiveness in improving the mechanical reliability of Cu/low-k interconnect. The study also illustrated that the crack driving force increased with the crack length. Therefore, the most effective way to use the crack stop concept is to embed it close enough to the location where cracks initiate such as the die edge or where the fully dense low-k material contacts with the ultra low-k material.

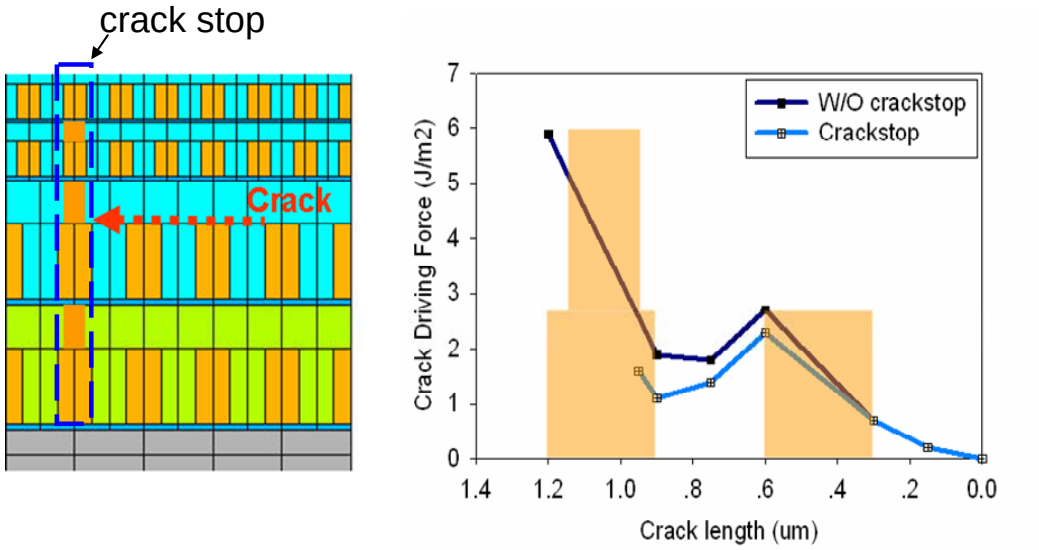


Figure 4.18: Effect of crackstop structure on ERR

A Modified Edge Liftoff Test (m-ELT) was used to determine the effect of fracture toughness of crack-stop structures built into the Cu/low-k interconnects [37, 38]. To prepare the specimen, a thick layer of epoxy was deposited on top of Si wafer and then cured for one hour at 177^{o}C (Figure 4.19). After curing, the sample was diced into 1 cm x 1 cm coupons. Then these diced specimens were placed in a sealed chamber with liquid nitrogen to cool down until the epoxy started to peel off from the wafer. The temperature at which debonding occurred was recorded and the corresponding residual stress can be extrapolated using a calibrated residual stress vs. temperature curve. The strain energy release rate can be calculated by Eq. 4.5 [37, 38].

Figure 4.19: Schematics of m-ELT sample

$$G_c = \frac{\sigma_e^2(T)\cdot h}{2\overline{E}_{film}}$$
$$\overline{E}_{film} = \frac{E_{film}}{1-\nu^2} \qquad (4.5)$$

where σ_e is the residual stress in the epoxy coating layer; h is the epoxy thickness and E and v are Yong's modulus and Poisson's ratio.

Several crack stop designs were tested using m-ELT technique and the results are plotted in Figure 4.20. Significant increases in the fracture resistance were observed for chips with crack stop structures to about 20 J/m^2 as compared with chips without crack stop structures, usually about 1~4 J/m^2 [8]. This demonstrated the effectiveness of the crack structure in preventing cracks from propagating in the interconnect structure. Failure analysis of these samples yielded a crack propagation path from the global interconnect level to the local level as shown in Figure4.21, which confirmed the previous simulation results.

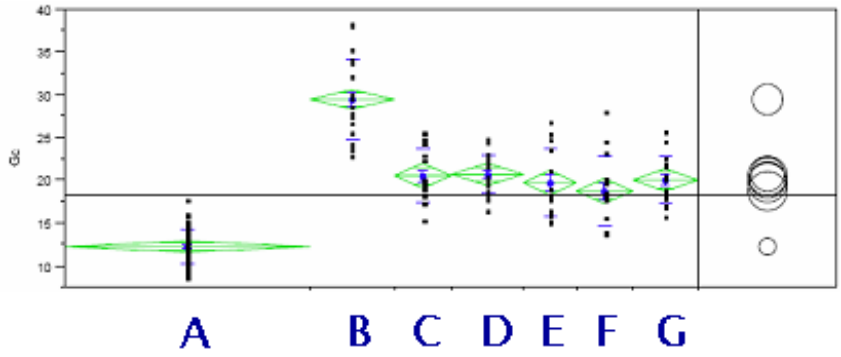


Figure 4.20: Fracture toughness measurement of crackstop by m-ELT

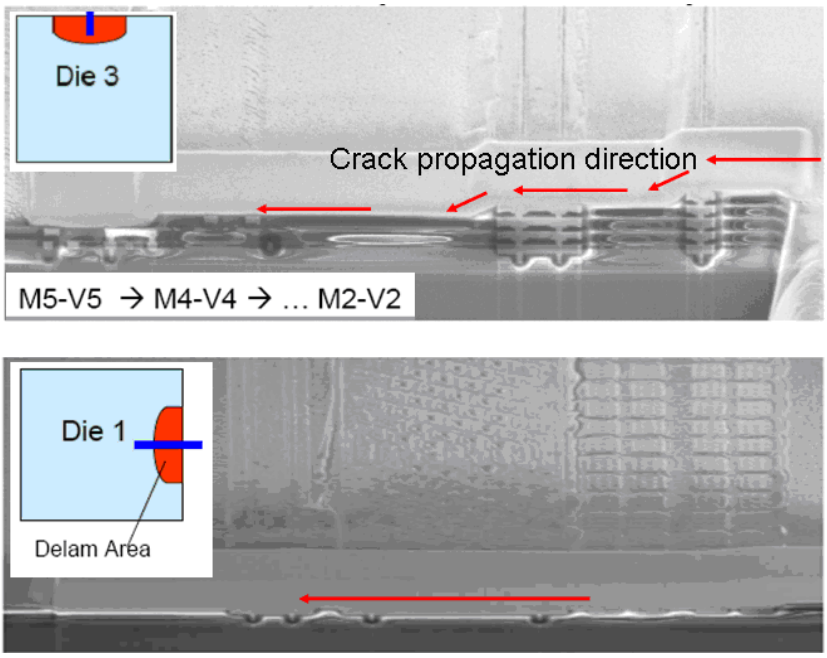


Figure 4.21: Failure analysis of failed samples [35]

Crack stop structures have attracted a lot of attentions from the semiconductor industry and research institutes. Many process and structural optimizations have been advanced to improve the Cu/low-k reliability. Figure 4.22 illustrated the competition between the crack driving force and fracture toughness of crackstops. The crack driving force for low-k dielectric fracture increases with crack length quickly at the beginning stage and then slowly flattens. The yellow vertical bar represents the fracture resistance of crack stop structures. If the fracture resistance of crack stop is larger than the crack driving force, the crack growth will be halted. Otherwise, the crack will penetrate through the crack stop structure. Therefore, the location of the crack stop structure is quite crucial. The most effective way is to embed the crack stop as close as possible to the crack initiation points. Liu and Shaw [8] from IBM reported that certain crack stop designs were not very effective in preventing the dicing defects from propagating into the die

because of the long distance from the die edge to the crack stop. Besides the location of the crack stop, the fracture resistance of the crack stop structure and low-k dielectrics is also very important. More resistance means less susceptibility to fracture and larger process margin. In addition, several other techniques have been proposed to improve the mechanical reliability of low-k interconnect including optimization of the dicing process [39] and repair of dicing defects based on chemical reaction [40].

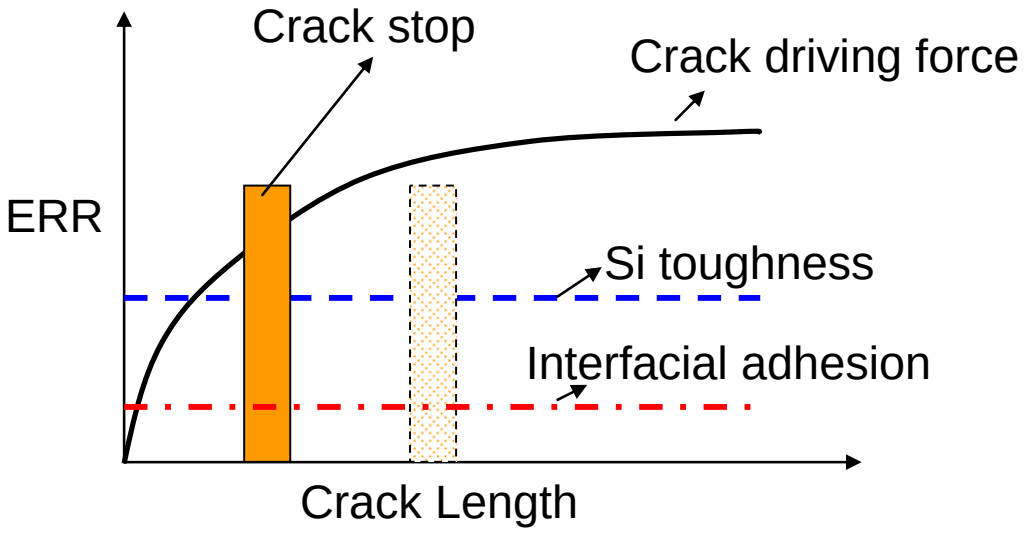


Figure 4.22: Effect of crack stop in suppressing crack growth [8]

4.9 Summary

In this chapter, chip-package interaction and its impact on Cu/low-k interconnect reliability were investigated. The origin of the problem was traced to the weak thermomechanical properties of the low-k dielectric material and the large thermal stress induced by package deformation during packaging processes to drive crack propagation. The nature of interfacial delamination and crack growth in multilayered dielectric

structures was discussed based on fracture mechanics. The chip-package interaction was investigated using 3D finite element analysis (FEA) based on a multilevel sub-modeling approach. The packaging induced crack driving force for relevant interfaces in Cu/low-k structures was deduced. The die attach process was found to be a critical step and the energy release rate was found to depend on the material properties of solder and low-k dielectrics. The implementation of lead-free solder and ultra low-k material poses great threats to the mechanical stability of the Cu interconnect due to the increased driving force for fracture. Structural optimization such as changing the geometry and structural layout at both package level and interconnect level were found to be effective in retaining the mechanical reliability of Cu/ultra low-k interconnects under CPI. The crack propagation in low-k interconnect driven by CPI was then analyzed. Simulation results demonstrated that the crack would propagate from the global-level interconnect towards Si substrate under CPI, which agreed well with the experimental observations. A decrease in the energy release rate can be achieved by adding dummy Cu structures into the low-k interconnect. Meanwhile, m-ELT results revealed that the fracture resistance of the structure was increased by implementing crackstops. Nevertheless, as discussed in the last section, a proper layout and design of the crackstop structure is critical in order to effectively suppress crack propagation and improve the mechanical reliability of Cu/ultra low-k interconnect.

Chapter 5: Thermo-Mechanical Reliability Challenges of 3-D Integration with TSVs

5.1 Introduction

Three-dimensional (3D) integrated circuits with through silicon vias (TSVs) has emerged as a promising approach to improve the device density without continuous down-scaling of the interconnect structure. Such 3D structures enable shorter interconnection paths for better electrical performance and heterogeneous integration of different subsystems such as logic devices and digital circuits. This has stimulated extensive efforts recently to develop the design and processing of 3D interconnects with TSVs. The basic manufacturing process consists of a deep reactive ion etching or laser drilling of the silicon substrate, deposition of electrical isolation and diffusion barrier layers, deposition of a Cu seed layer, and Cu metallization. The via configuration and process sequence (via first or via last) vary with the TSV materials and geometries. Polysilicon, tungsten, and copper are commonly used for via filling, among which copper has the advantage of having a low resistivity. Various via filling technologies have been developed for Cu TSV in which Chemical vapor deposition (CVD) process is preferred for small vias with diameter less than 5μm while electroplating is favored for vias with a diameter larger than 5μm [1]. Various process optimizations have been proposed to optimize the fabrication process of 3D interconnects, including deep silicon etching and optimized seed layer and electroplating profile [1].

On the other hand, only a few studies have been reported on the thermo-mechanical reliability of 3D interconnect structures so far. Stress evolution in 3D

interconnects during fabrication can be traced to the CTE mismatch between the Cu TSV and Si with Cu being 6-7 times higher. Ramm [2] reported a higher residual stress for Cu-filled TSVs compared with tungsten-filled TSVs. Additionally, the thin die (25-100 μm) and the high aspect ratio (>5:1) of TSV can lead to a complex stress state which may be sufficient to drive crack and interconnect failure [3, 4]. The process-induced thermal stresses can also impact the performance of stress-sensitive devices. Thompson reported that in-plane stresses of only 100 MPa can degrade the mobility in device by up to 7.2% [2]. The stress-related problem has necessitated the design of a proper keep-away zone for devices around the TSVs. Such reliability issues need to be addressed in order to develop reliable 3D interconnects.

In this chapter, the study of the thermo-mechanical reliability of 3D interconnects with electroplated Cu TSVs is organized in two parts. First the study of the process-induced residual stress and the keep-away zone design are reported. This is followed by a fracture analysis of 3D interconnects with Cu TSVs.

In the first part, the residual stresses in TSV structures are calculated by finite element method. The properties of copper required for FEA modeling are obtained experimentally using a dynamic mechanical analysis (DMA) and bending beam technique [5]. Various TSV configurations with different via diameters, Cu fill ratios, and pitch-to-diameter ratios, etc. are investigated and compared. Guidelines for structural optimization to minimize the process-reduced residual stress are discussed.

In the second part, the fracture behavior of the TSV structure is studied. Analytical solutions are deduced and three probable failure modes are investigated including silicon z-cracking, silicon r-cracking, and interface debonding between the

TSV and silicon matrix. The corresponding energy release rate and critical crack stress are deduced and compared to the fracture toughness of silicon and adhesion of TSV/silicon interface. Design guidelines of 3D interconnects with TSVs to improve thermal mechanical reliability are presented.

5.2 Process-induced residual stress and keep-away zone design

The thermal stresses of a 2X2 TSV array (Figure 5.1) was investigated by use of FEA. Process-induced thermal stresses in the Si matrix were calculated by employing the element birth and death technique [2]. A simplified fabrication process for TSV interconnects (Figure 5.2) was used in the simulation. The process started with a TEOS oxide layer deposition at 400^{o}C with thickness varying from 0.15 to 0.5μm. This was followed by the deposition of a thin barrier layer and a seed layer at 400^{o}C. The barrier thickness varies with the TSV diameter. After the barrier deposition, copper was electroplated at room temperature and then heated to 200^{o}C. Finally the whole structure was cooled down to room temperature [1].

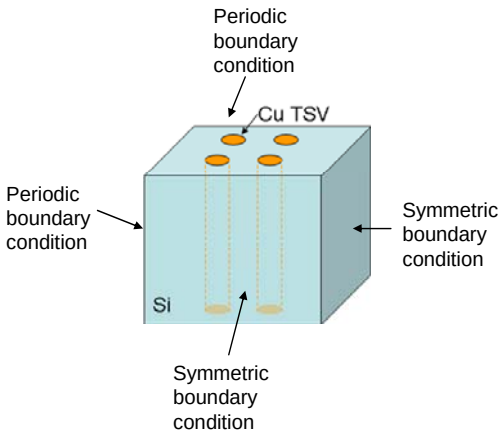


Figure 5.1: FEA model of TSV interconnect

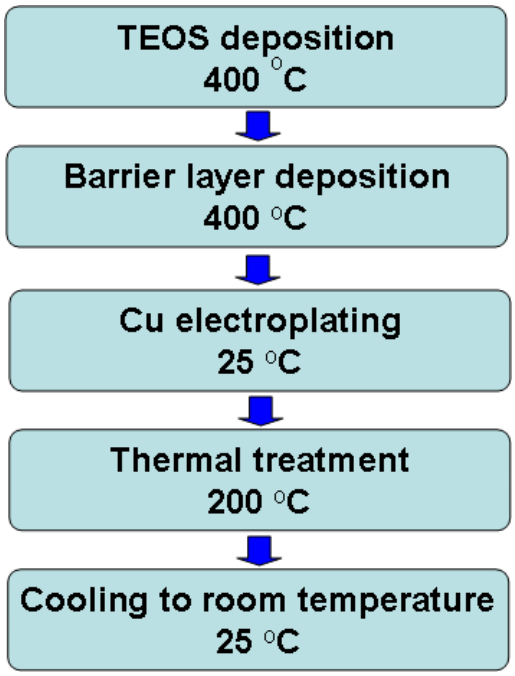


Figure 5.2: Simplified process for thermal simulation

Thermal stresses were developed during the fabrication process due to the CTE mismatch in constituent materials. According to the simulation results, large stresses were built up in the TSV structure when heating the sample to the thermal treatment temperature after Cu electroplating. These stresses may be sufficient to induce silicon r-cracking and interface debonding between the Cu TSV and the silicon matrix, which will be discussed in the second part of this chapter. After cooling down to room temperature, the TSV structure will still have a final stress in the structure as shown in Figure 5.3. The location of the maximum stress in silicon was found to be very close to the Cu TSVs and the stress gradually decayed away from the TSVs. The distribution of the residual stresses is important for designing the keep-away zone for devices.

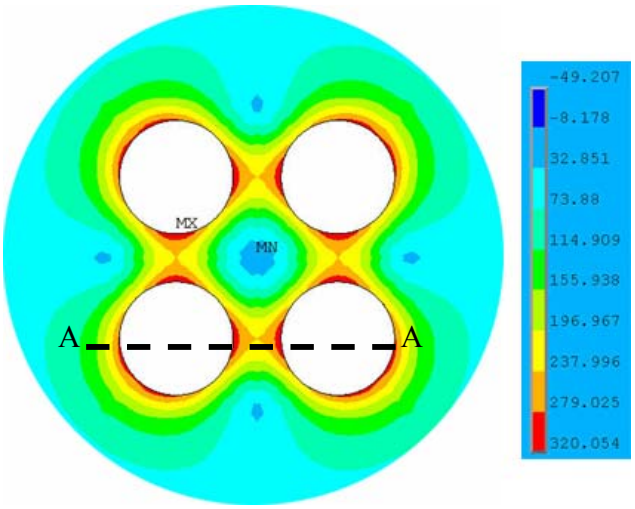


Figure 5.3: Residual radial stress distribution in TSV interconnects at top surface

In this study, 3D interconnects with various TSV geometries and configurations were investigated in order to find the optimized structural design. Figure 4 shows the stress components in which the radial and hoop stresses in silicon at the surface are the dominant components and thus are important in defining the keep-away zone. We first studied the effect of TSV diameter on the process-induced stresses, which was followed by the analysis of Cu filling ratio and TSV aspect ratio. The radial stress distributions at the top surface, along the path A-A in Figure 5.4 over the two adjacent TSVs were plotted in Figure 5.5 for three different TSV diameters; 5, 10, and 15µm, but with a fixed pitch of 20 µm. A significant increase in the radial stress was observed as the TSV diameter increased from 5 µm to 15 µm. The maximum radial stress increased by nearly a factor of two and the area affected by the residual stress in silicon was enlarged as well.

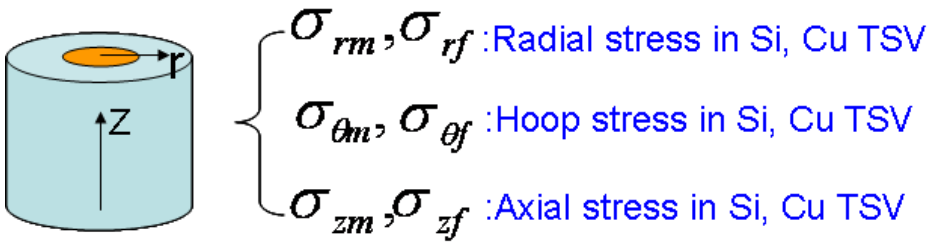


Figure 5.4: Stress components

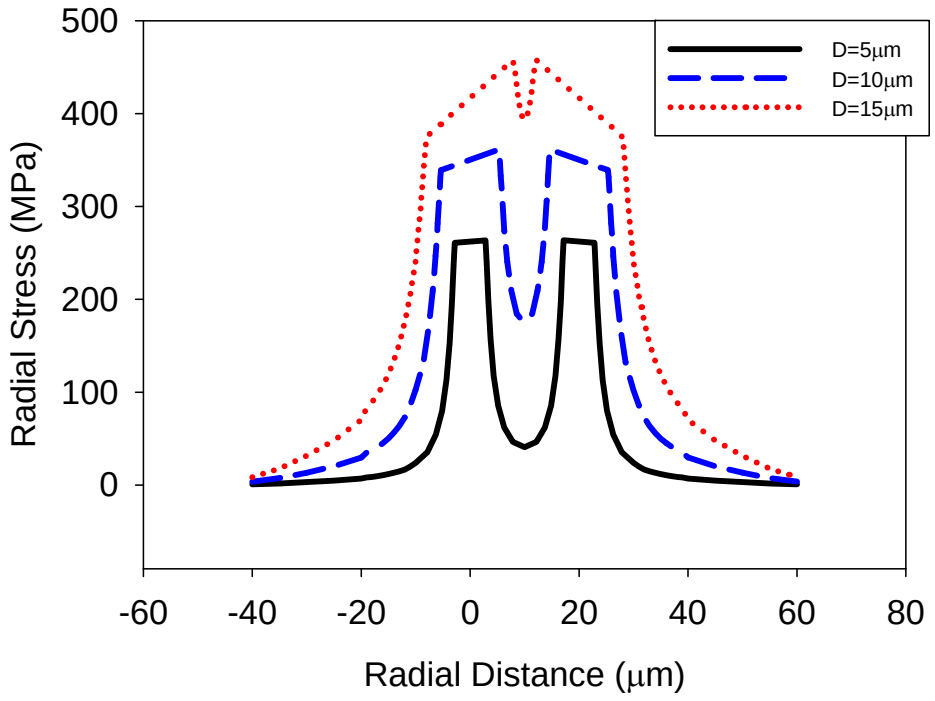
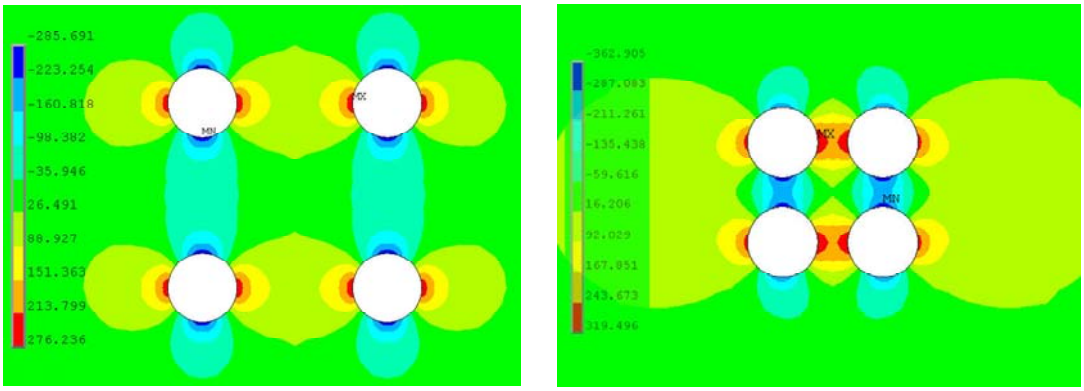


Figure 5.5: Radial stress distribution over two adjacent TSVs along the path A-A in Figure 5.4 as a function of TSV diameter at a fixed pitch

Figure 5.5 also demonstrated the effect of stress intensification in the TSV array due to overlapping of the stress field of each TSV. For example, for the case with 15μm TSV, the stress gradient in the Cu TSV illustrated the stress field overlapping of adjacent

TSVs in the center region. To study this stress field interaction, two TSV arrays with the same diameter but different pitch-to-diameter ratio were compared and their stress distributions were plotted in Figure 5.6. Significant stress enhancement was found in structures with smaller pitch-to-diameter ratio. The maximum normal stress of silicon increased from 275 MPa to 320 MPa, which would impact the keep-away zone shape and increase the hazard of silicon cracking as well. The pitch-to-diameter ratio for TSVs is an important parameter in the keep-away zone design. The simulation results demonstrated that the intensification of the maximum normal stress can be reduced when the pitch-to-diameter ratio is greater than two. Therefore, a minimum pitch-to-diameter ratio of two was proposed in this study as a minimum limit to avoid significant stress enhancement among adjacent TSVs.



Cu TSV diameter = 5µm
Pitch=15µm

Cu TSV diameter = 5µm
Pitch=8µm

Figure 5.6: Effect of pitch-to-diameter ratio on in-plane normal stress distribution in 3D interconnects

To separate the geometric effect from the stress field interaction between the adjacent TSVs, a single TSV in silicon matrix was analyzed. The effect of TSV diameter

on the magnitude of the thermal residual stress after fabrication was summarized in Figure 5.7. The values of all stress components were reduced as the TSV diameter became smaller except for the axial stress in Cu TSV which increased slightly. This indicated that the process-induced residual stress in silicon can be effectively mitigated by reducing the Cu TSV diameter.

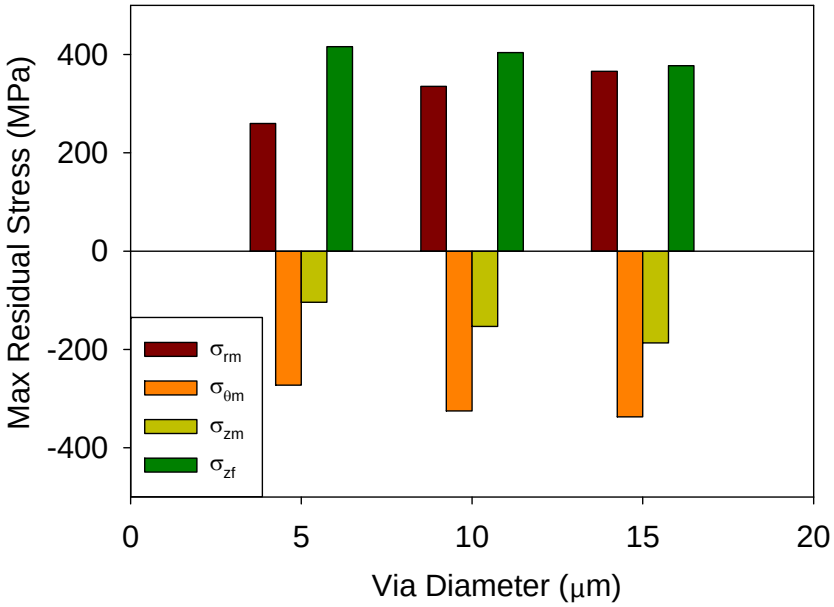


Figure 5.7: Effect of TSV diameter on the stress distribution in 3D interconnects

Another way to reduce the residual stress is to decrease the Cu filling ratio. Our simulation results indicated that, by replacing solid Cu TSV with hollow structures, the stress level in both silicon and Cu TSV can be reduced by as much as a half. The comparison between three different filling conditions, complete fill (solid Cu TSV), half fill and a quarter fill (hollow Cu TSV) were shown in Figures 5.8 and 5.9(a)

Besides TSV diameter and Cu fill ratio, other variables such like Cu volume ratio, thickness of SiO_2 isolation layer and TSV aspect ratio also have strong effects on the thermal residual stress. Increasing the Cu volume ratio reduces the radial stress which benefits the design of the keep-away zone (Figure 5.9(b)). However, a silicon substrate with a dense metal configuration is more prone to r-cracking due to the increase of hoop stress in silicon which will be shown in the fracture study. Meanwhile, the axial stress in silicon increases with metal density and is detrimental to the silicon integrity. In comparison, an increase in the thickness of buffer layer between Cu TSV and silicon can effectively reduce the magnitude of all the stress components in silicon and Cu TSV as shown in Figure 5.9(c). Thus the implementation of SiO_2 or soft polymer layers between Cu TSV and silicon can buffer the CTE mismatch between Cu and silicon. The effect of these parameters on residual stress in 3D interconnect are summarized in Table 5.1 where the plus sign denotes increase in the stress level while the negative sign means the opposite. The largest changes were highlighted by red color for each column. The results indicated that the via diameter and the Cu filling ratio have the largest impact the radial and hoop stresses and therefore the keep-away zone design while the via diameter and the Cu volume ratio dominate the magnitudes of axial stresses and interface stresses which are important in controlling the Si fracture and interface debonding.

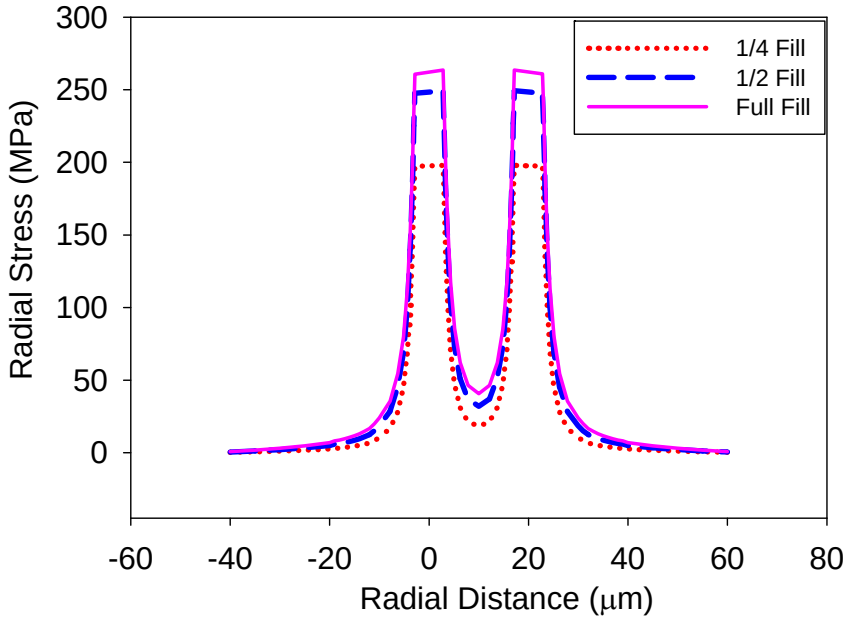
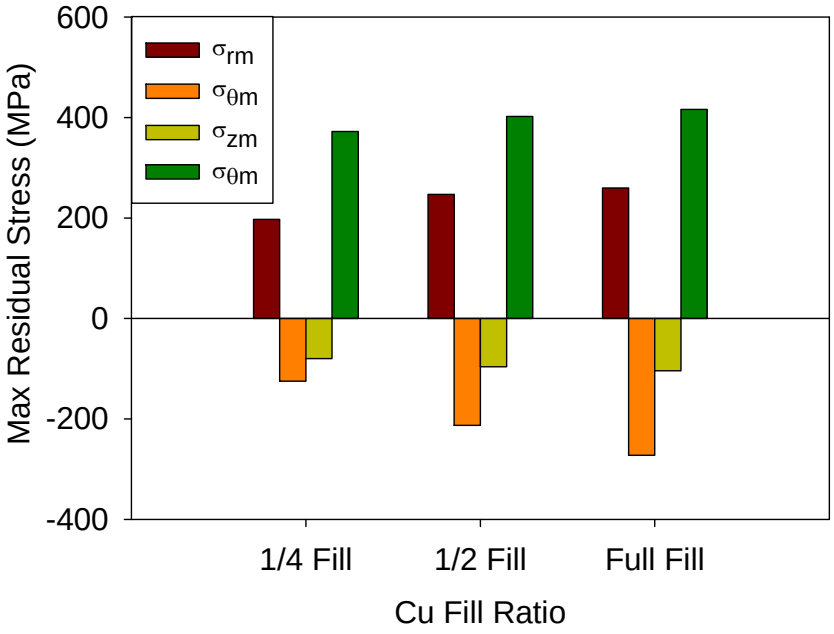
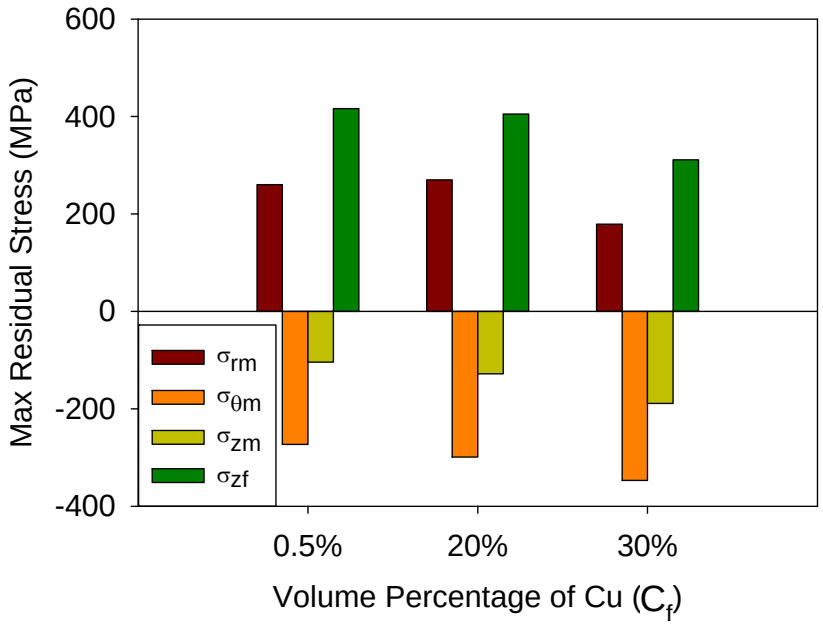


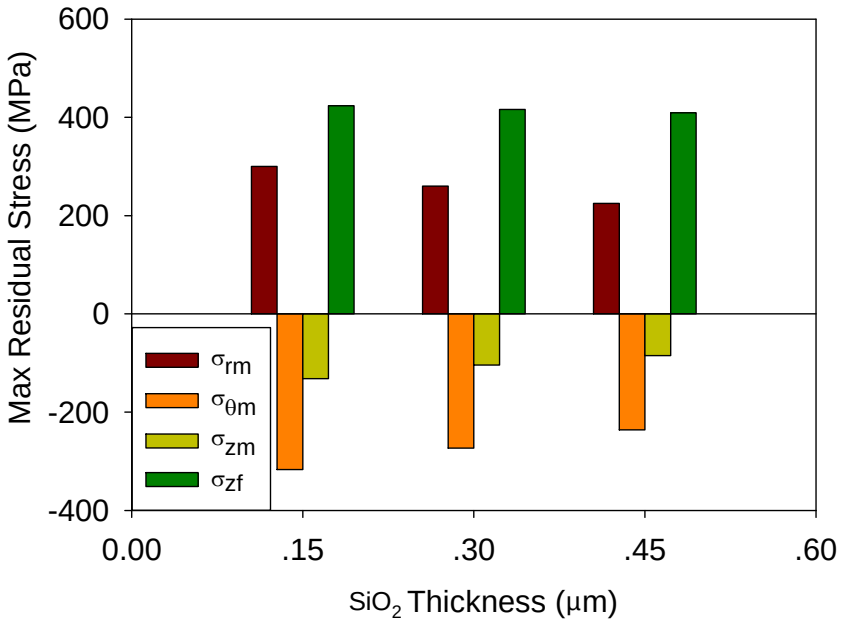
Figure 5.8: Radial stress distribution in silicon as TSV fill ratio



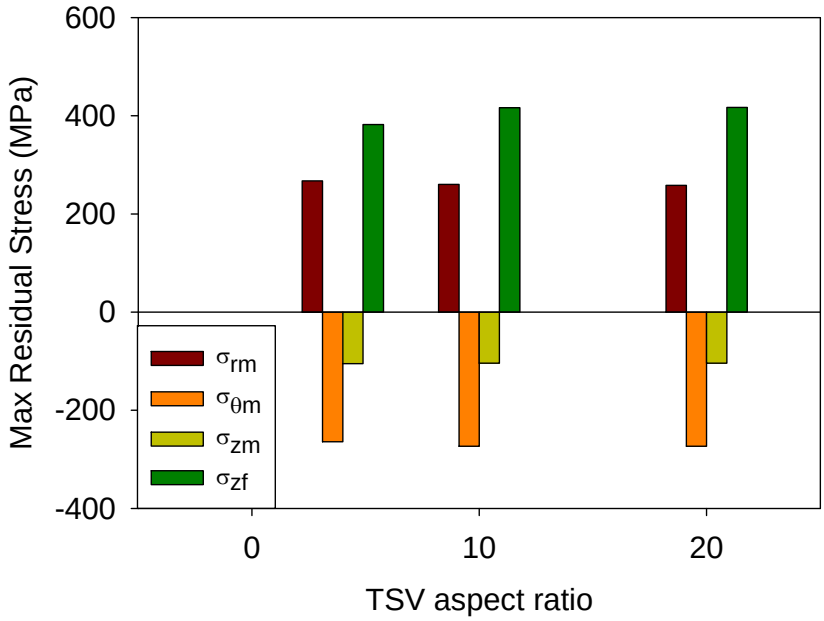
(a)


600
400
200
0
-200
-400
Max Residual Stress (MPa)
σrm
σθm
σzm
σzf
0.5%
20%
30%
Volume Percentage of Cu (Cf)

(b)


600
400
200
0
-200
-400
Max Residual Stress (MPa)
σrm
σθm
σzm
σzf
0.00
.15
.30
.45
.60
SiO2 Thickness (μm)

(c)



(d)

Figure 5.9: Effect of (a) TSV fill ratio (b) Cu volume ratio (c) SiO_2 thickness (d) TSV aspect ratio on stress distribution in 3D interconnects

Table 5.1: Effect of TSV configuration on residual stress

Max stress / Parameter	σ_{rm}	$\sigma_{\theta m}$	σ_{zm}	σ_{zf}
Via diameter: *5μm to 15μm*	+41%	+24%	+80%	-9%
Cu fill ratio: *Full fill to ¼ fill*	-24%	-54%	-23%	-11%
Cu volume ratio: *0.5% to 30%*	-31%	+27%	+82%	-25%
TSV aspect ratio: *4 to 20*	-3%	+3%	-1%	+9%
SiO_2 thickness: *0.15μm to 0.45μm*	-25%	-26%	-35%	-3%

5.3 Fracture analysis of 3D interconnect with Cu TSVs

The process-induced residual stress not only impacts the device performance but also raises mechanical reliability issues in the 3D interconnect by driving cohesive cracking in silicon and delamination at TSV interfaces. In addition, after TSV fabrication, the 3D interconnects are subjected to various thermal and mechanical loads during wafer thinning, handling, bonding processes, and subsequent thermal cycling. So far, only limited information has been reported on the failure mechanisms of 3D interconnect with TSVs.

In this section fracture analysis was performed to understand these reliability problems. Several possible failure modes can be predicted based on the thermal stress analysis by considering the locations of the stress concentration. Moreover, the Cu TSV/Si matrix system is analogous to the classical fiber-reinforced composite which has been well studied [6, 7]. Some of the previous analysis can be modified and applied to the thermo-mechanical reliability study of 3D interconnects. Three failure modes were proposed and investigated including silicon matrix r-cracking, silicon matrix z-cracking, and interface debonding between TSV and silicon as shown in Figure 5.10 [6, 7].

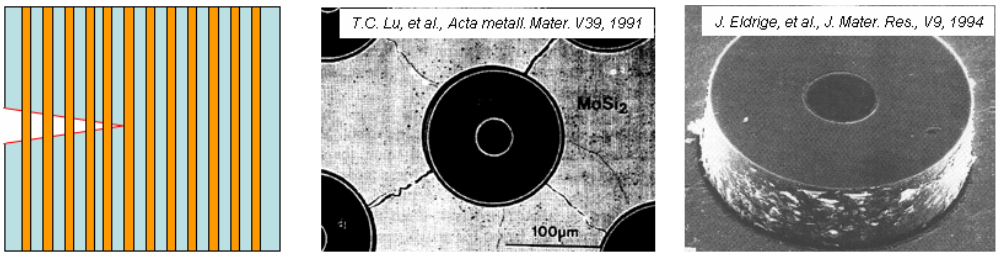


Figure 10. Failure modes for 3D interconnects with Cu TSVs, I. z-crack, II. R-crack [taken from [6]], and III. Debonding and pull out [taken from [7]].

In order to analyze the fracture behavior of the 3D interconnects, the stress components in both silicon and Cu TSV are required. Therefore, we first derived an analytical solution for a unit cell of Cu TSV/silicon system as shown in Figure 5.11.

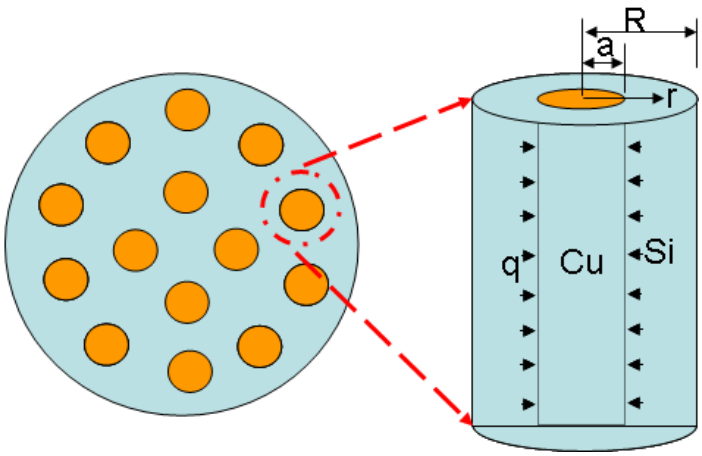


Figure 5.11: Unit cell of Cu TSV/Si system for stress analysis

By conforming to the displacement compatibility at the interface, the clamping force at the Cu/Si interface can be obtained by Eq. 5.1

$$q = \frac{\Delta\alpha\Delta T}{\frac{C_f(1-2\nu_m)+1}{E_m C_m} + \frac{1-2\nu_f}{E_f}} \qquad (5.1)$$

And the corresponding stress distribution in Cu TSV and silicon matrix was deduced as shown in Eq. 5.2 and 5.3. By ignoring the surface effect, the following stress components can be obtained.

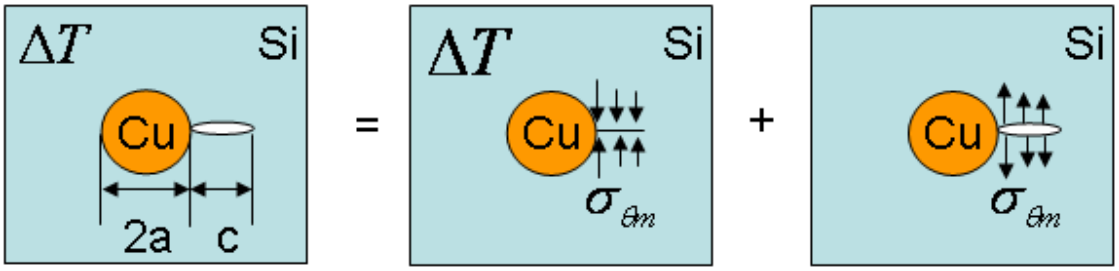
$$\text{For Cu} \begin{cases} \sigma_{rf} = -q \\ \sigma_{\theta f} = -q \\ \sigma_{zf} = -\dfrac{C_m}{C_f} * \sigma_{zm} \end{cases} \qquad (5.2)$$

$$\text{For Si} \begin{cases} \sigma_{rm} = \dfrac{q}{1-C_f}(C_f - \dfrac{a^2}{r^2}) \\ \sigma_{\theta m} = \dfrac{q}{1-C_f}(C_f + \dfrac{a^2}{r^2}) \\ \sigma_{zm} = \left[\Delta\alpha\Delta T + \dfrac{2\nu_f q}{E_f} + \dfrac{2\nu_m q C_f}{E_m(1-C_f)}\right] / \left(\dfrac{C_f E_f + C_m E_m}{E_m E_f C_f}\right) \end{cases} \qquad (5.3)$$

where C_m and C_f are the volume ratio of silicon and Cu, respectively. E_f and V_f are the Young's modulus and Poisson's ratio of Cu, E_m and v_m are Young's modulus and Poisson's ratio of silicon. $\Delta\alpha$ is the CTE difference, and ΔT is the thermal load.

5.3.1 Silicon r-cracking

The first fracture mode studied is silicon r-cracking in which the crack propagates along the radial direction under mode 1. The stress intensity factor for crack propagation induced by thermal stress was calculated by a superposition method as depicted in Figure. 5.12.



Case I Case II Case III

Figure 5.12: Stress intensity factor calculation for r-crack

For a single TSV in infinite silicon matrix, the stress intensity factor K_I can be deduced using the following equation [8];

$$K_I = \int_a^{a+c} \sigma_\theta(r) \sqrt{\frac{2}{\pi c}} \sqrt{\frac{r-a}{c+a-r}} dr \qquad (5.4)$$

where a is the TSV radius and c is the initial defect length. Substituting $\sigma_\theta(r)$ from the previous analytical solution into Eq. 5.4, K_I was simplified to Eq. 5.5.

$$K_I = \left(\frac{\Delta\alpha\Delta T}{\frac{1}{E} + \frac{1-2\nu_f}{E_f}} \right) \sqrt{\frac{\pi}{2}} \sqrt{\frac{c}{a}} \frac{a^2}{(a+c)^{3/2}} \qquad (5.5)$$

where $E=C_f*E_f+C_m*E_m$

For a system containing multiple TSVs (Figure 5.13), each TSV contributes to the stress intensity factor for the crack. The effect of surrounding TSVs close to TSV #1, where a crack has initiated, also needs to be considered in the overall stress intensity factor. In this study, TSV #1 and #2 were included in the K_I calculation while the contributions from other adjacent TSVs were neglected because they were further away from the pre-crack and had little impact on the K_I [6].

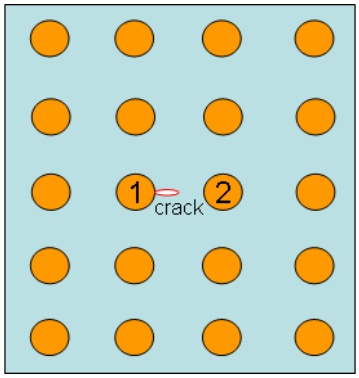


Figure 5.13: Stress intensity factor calculation for r-crack in a TSV array

The stress intensity factor from TSV #2 can be calculated with the following equation [8],

$$K_I = \left(\frac{\Delta\alpha\Delta T}{\frac{1}{E} + \frac{1-2\nu_f}{E_f}} \right) \sqrt{\frac{\pi}{2}} \sqrt{c} \frac{a^2}{\sqrt{(R-a)}\sqrt[3]{(R-a-c)}} \qquad (5.6)$$

The total stress intensity factor K_I consists of contributions from both TSV #1 and #2 and is a function of Cu via diameter, Cu volume ratio, crack size and thermal load.

$$K_I = \left(\frac{\Delta\alpha\Delta T}{\frac{1}{E} + \frac{1-2\nu_f}{E_f}} \right) \sqrt{\frac{\pi}{2}} \left(\sqrt{\frac{c}{a}} \frac{a^2}{(a+c)^{3/2}} + \sqrt{c} \frac{a^2}{\sqrt{(R-a)}\sqrt[3]{(R-a-c)}} \right) \quad (5.7)$$

where R is the pitch of TSV array. The energy release rate of the crack can therefore be deduced by Eq. 5.8.

$$G = \frac{K_I^{\,2}}{E}\left(1-\nu^2\right) \quad (5.8)$$

A plot of G for c/a=0.5 and $\Delta T=175^oC$ is shown in Figure 5.14. The parameter G provides a measure of the tendency for the crack to grow. This tendency needs to be compared with the silicon toughness G_{IC} which determines whether the crack will propagate or stagnate. Table 5.2 listed the silicon toughness G_{IC} along the different silicon directions. If the calculated G is larger than G_{IC}, the initial crack will start to grow. The results demonstrated that for small vias with a radius of less than 5 μm, the energy release rate for r-crack propagation was less than or comparable to the fracture resistance of silicon. However the crack driving force increased with via diameter quickly, especially for the case with a high Cu volume ratio. The maximum driving force can reach up to 26 J/m^2 for a radius of 50 μm, which is much larger than the silicon fracture resistance, indicating serious fracture issues in the structure.

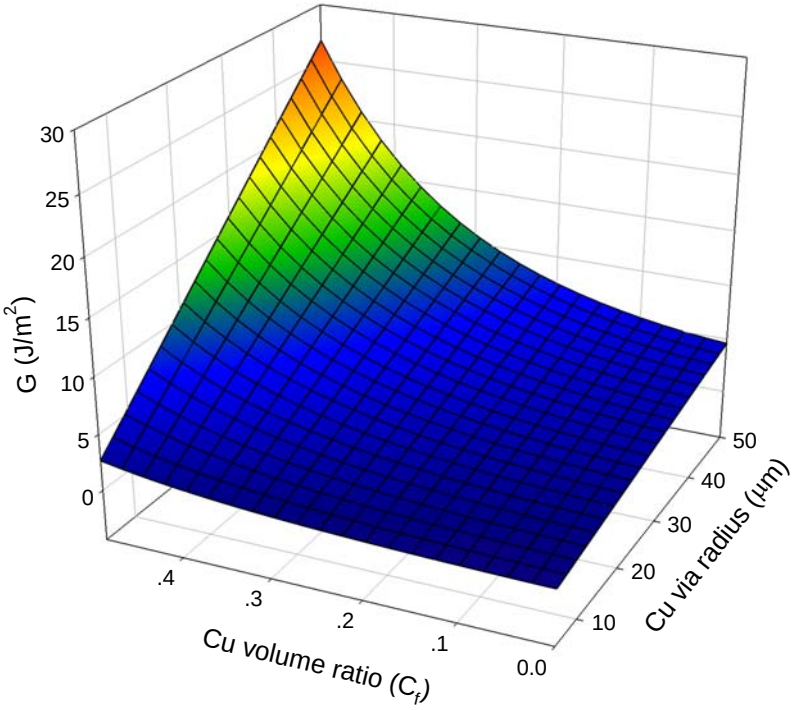


Figure 5.14: Stress intensity factor for silicon r-cracking

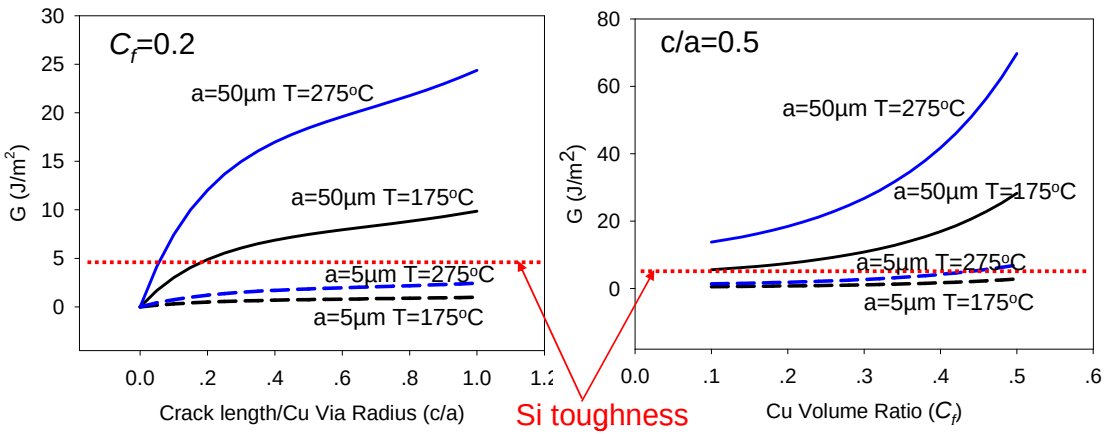
Table 5.2: Fracture toughness of Silicon

Si Direction	K_{IC} (MPa $*m^{1/2}$)	G_{IC} (J/m^2)
<111>	0.83 to 0.95	4 to 5.3
<100>	0.91	4.9
<110>	0.94	5.2
Polycrystalline Silicon	0.94	5.2

In Figure 14, the Cu volume ratio only extends to 0.5. This is because of the geometric constraint, pitch>2a+c (Figure 5.13). The relation between C_f and c/a can be expressed by Eq. 5.9 after proper manipulations. When c/a equals 0.5, C_f is less that 0.5.

$$\sqrt{\frac{\pi}{C_f}} \geq 2 + \frac{c}{a} \qquad (5.9)$$

Comparison among four cases of r-crack with varying TSV diameters and thermal loads are shown in Figure 5.15. The results dictated that the TSV with a larger diameter generated a larger crack driving force and the driving force also increased with the thermal load. Moreover, G increased as the Cu volume ratio increased for all four cases. Therefore, smaller via diameter and smaller Cu volume ratio are preferred to improve the resistance of 3D interconnect to silicon r-cracking.



(a) (b)

Figure 5.15: Comparison of G for various via sizes and thermal loads, with respect to (a) the crack length at a fixed Cu volume ratio, C_f=0.2, and (b) the Cu volume ratio at a fixed crack length, c/a=0.5

5.3.2 Interface debonding between Cu TSV and silicon matrix

Interface debonding between TSV and silicon is another important failure mode. Cu TSV tends to shrink or expand more than silicon under a given thermal load due to the CTE mismatch. Large thermal stress can develop at the interface, raising concerns of interfacial debonding and the TSV popping-out. Figure 5.16 shows a schematic of the interface debonding between TSV and silicon.

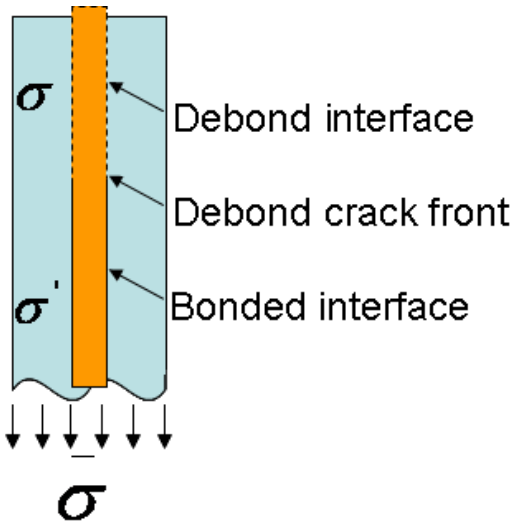


Figure 5.16: Schematic of interface debonding between TSV and silicon

As the crack front propagates downwards from debonding interface, the stress state near the crack front changes with the growth of the crack. In this case, the steady-state strain energy release rate for crack propagation equals to the interfacial adhesion strength. Hutchinson et al. [8] analyzed the debonding energy release rate for a fiber embedded in a brittle matrix. The same analysis can be applied to the Cu TSV in silicon substrate. Accordingly, the steady-state energy release rate for the interfacial debonding in the absence of friction is

$$G = E_m a\left[c_1 \frac{\bar{\sigma}}{E_m} + c_2 \varepsilon^T \right]^2 \qquad (5.9)$$

where $c_1 = \left[(1-\nu^2)(1-C_f)\right]^{1/2}/(2C_f)$, $c_2 = \frac{1}{2}\left[(1-C_f)/(1-\nu^2)\right]^{1/2}(1+\nu)$.

($0<C_f<1$). Given the interfacial adhesion, the critical stress for interface debonding can be deduced. In the case of pure thermal load, $\bar{\sigma} = \sigma_f C_f + \sigma_m C_m = 0$.

Figure 5.17 shows the energy release rate G as a function of Cu volume ratio and TSV radius for a thermal load of 175°C.

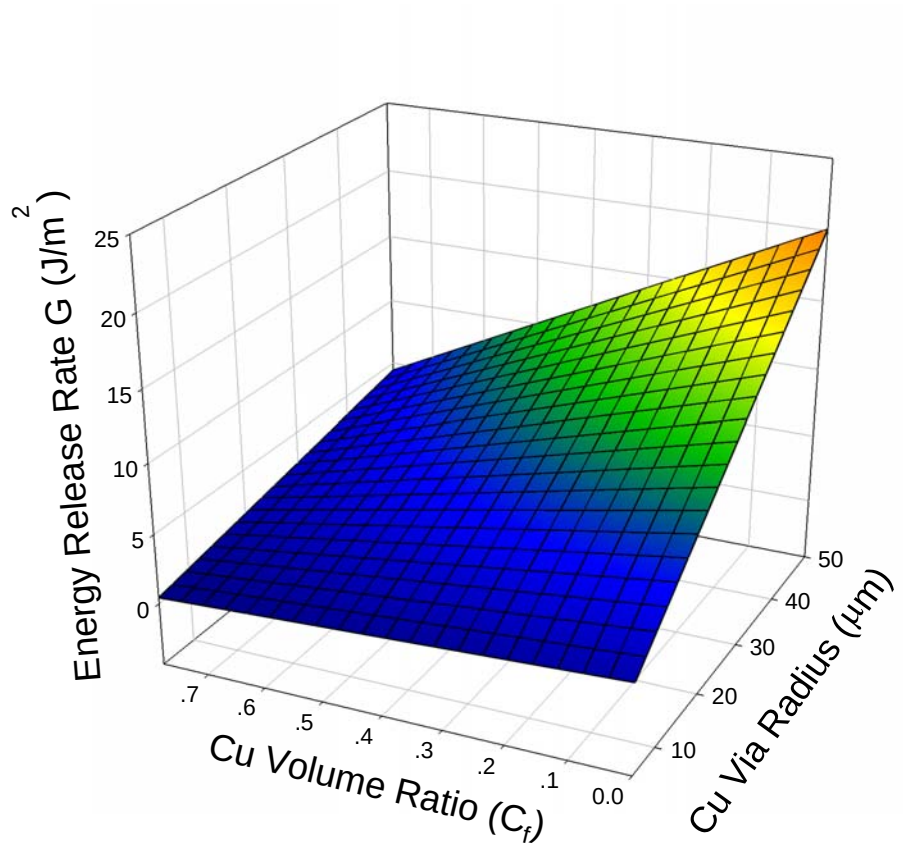


Figure 5.17: Energy release rate for debonding between Cu TSV and silicon

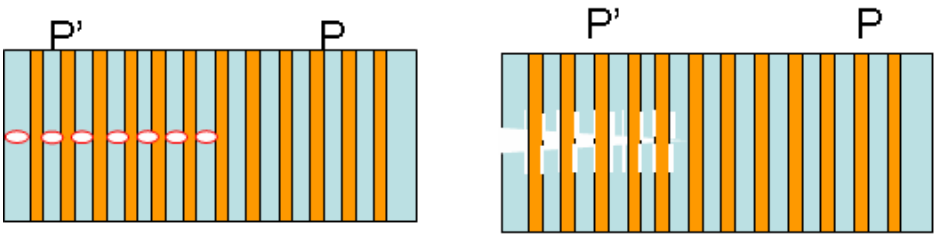
The energy release rate for interface debonding was found to increase rapidly with TSV radius and reach up to 20 J/m^2 at 50μm, indicating that TSVs with a larger radius are more prone to the TSV/silicon interface debonding. The adhesion strength of Cu to SiO_2 interface is in the range of 0.7 J/m^2 to 10 J/m^2 depending on the mode mixity [9]. Comparing the adhesion strength with the G values in Figure 5.17, it can be concluded that interface debonding and TSV pull out can indeed be a serious reliability problem for 3D interconnects with large Cu TSVs.

5.3.3 Silicon z-cracking

Another failure mode investigated is the silicon matrix z-cracking, which includes two cases as shown in Figure 5.18.

Case I: no debonding between Cu TSV and silicon, Figure 18(a)

Case II: with debonding and sliding between Cu TSV and silicon, Figure 18 (b)



(a) (b)

Figure 5.18: Silicon z-cracking failure mode (a) case I (b) case II

Similar to the case of TSV/silicon interface debonding, the z-cracking growth in silicon will change the potential energy in the system. If the potential energy is assumed to be P before cracking and P' after cracking, the potential energy release rate can be calculated by

$$G = \frac{P - P'}{\Delta S} . \qquad (5.10)$$

where ΔS is the crack advance distance. In case I, without debonding and sliding, the potential energy change is balanced only by the silicon cracking energy. Based on the energy balance, the critical stress for silicon z-cracking can be deduced by following Budiansky's method (Eq. 5.11) [10].

$$\sigma_{cr} = E_m B \left(\frac{6C_f^2 E_f}{C_m^2 E(1+\nu_m)} \right)^{\frac{1}{4}} \left(\frac{G_m}{aE_m} \right)^{\frac{1}{2}}$$

$$\mathrm{B} = \left[\frac{2\mathrm{C_m^3}}{-6\ln(\mathrm{C_f}) - 3\mathrm{C_m}(3 - C_f)} \right]^{\frac{1}{4}} \qquad (5.11)$$

$$E = E_m C_m + E_f C_f$$

where G_m is the fracture resistance of silicon, and a is the TSV radius.

The effect of TSV radius, a, and Cu volume ratio, C_f, on the critical stress for silicon z cracking is shown in Figure 5.19. The critical stress can reach 1 GPa for a perfect bonding case. The higher critical stress indicated that the system is more resistant to z-crack damage.

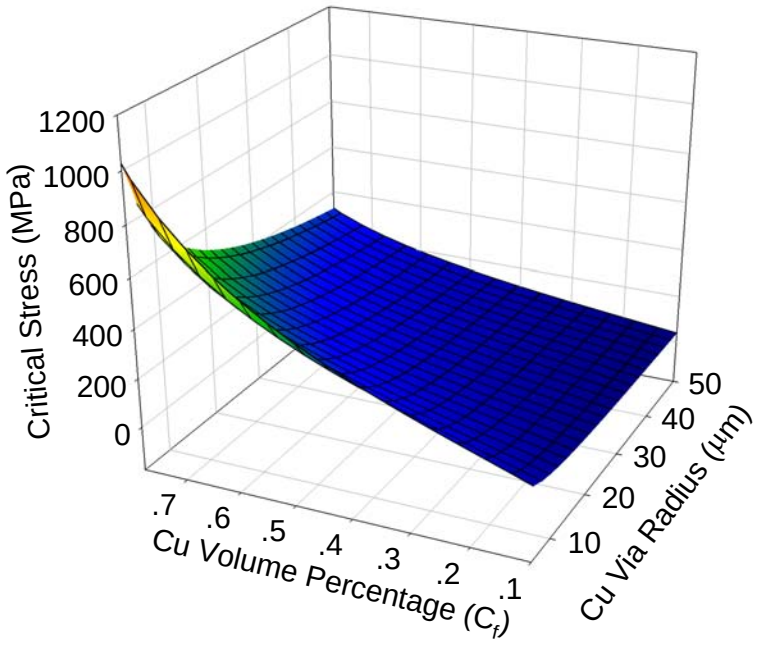


Figure 5.19: Critical stress for z-cracking failure with no debonding and sliding

In case II, the debonding and sliding between TSV and silicon are considered. In this case, the potential energy change in the system is balanced not only by the silicon crack energy release but also by the debonding energy release and frictional energy dissipation. Again, following Budiansky method, the critical stress for z-cracking can be calculated by the following equation 5.12 [10].

$$\sigma_{cr} = E_m \left(\frac{6\mu C_f^2 E_f}{C_m E_m E} \right)^{\frac{1}{3}} \left(\frac{G_m q}{a E_m} \right)^{\frac{1}{3}}$$
$$E = E_m C_m + E_f C_f \tag{5.12}$$

where μ is the friction coefficient between Cu TSV and silicon. A plot of the critical cracking stress for μ=0.1 is shown in Figure 5.20. Compared with case I, the critical stress for z-cracking was reduced to below 250 MPa when both debonding and sliding were considered.

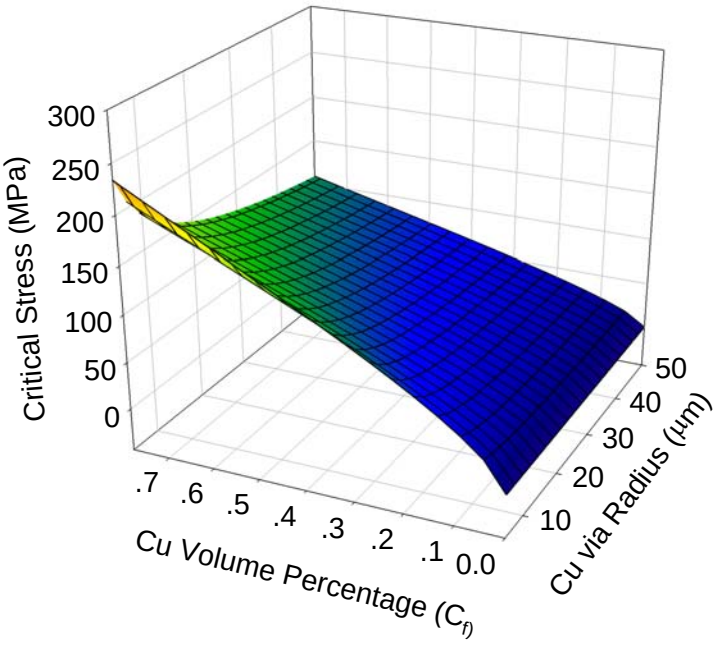


Figure 5.20: Critical stress for z-cracking failure with debonding and sliding

A detailed comparison between these two cases is given in Figure 5.21. The results clearly demonstrated that debonding and sliding between Cu TSV and silicon exacerbated silicon z-cracking by reducing the critical stress for crack growth. For both cases, the critical stress decreased as TSV radius increases, indicating silicon z-cracking problem is more critical for 3D interconnects with larger vias. In contrast, increasing the Cu volume ratio tended to increase the critical stress for z-cracking, making silicon more

resistant to z-cracking. According to our simulations and analytical analysis data, the thermal residual stress induced by TSV fabrication in 3D interconnects in general is not large enough to cause z-cracking in silicon. However, additional external loads will be applied to the z-direction in the structure during the wafer handling, bonding, and subsequent packaging process. The external loads may raise the likelihood of z-cracking in silicon and need to be carefully investigated in further study.

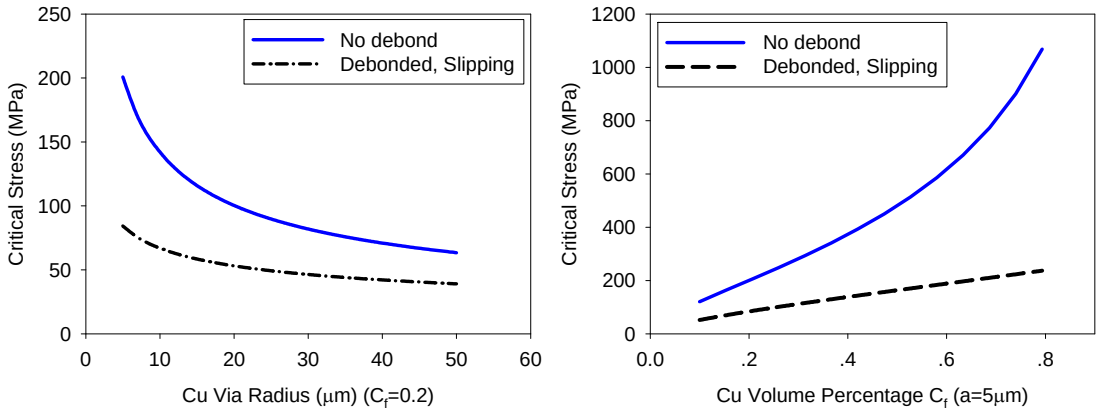


Figure 5.21: Comparison of critical cracking stress between two cases

The fracture analysis of 3D interconnect with TSVs under thermal stress enabled us to identify the most important parameters in designing the TSV structures and configuration. This study demonstrated that Cu TSV diameter is a key variable in controlling the mechanical stability of 3D TSV structure. TSVs with large diameter will induce larger crack driving force for silicon r-cracking and interfacial debonding. Cu metal density is another parameter that should be considered carefully in the design of 3D interconnects. Though increase of Cu volume percentage can improve the fracture resistance of silicon to z-cracking and reduce the energy release rate for Cu/TSV

interfacial delamination, it causes a substantial increase in the crack driving force for silicon r-cracking especially for 3D structure with large TSVs.

Interfacial debonding between Cu TSV and silicon is another critical concern for 3D interconnects. Strong adhesion strength at the interface can inhabit the debonding and prevent TSV extrusion. Meanwhile, strong interfacial adhesion can also substantially increase the critical stress for silicon z-cracking, making 3D interconnects more robust during wafer handling and packaging.

5.4 Summary

Finite element analysis (FEA) was employed to investigate the thermo-mechanical reliability of 3D interconnects containing Cu TSVs. In the first part of this chapter, process-induced residual stresses in TSV structures were calculated. Approaches to reduce the residual stress were discussed. Significant stress reduction can be achieved by optimizing the TSV geometry and configuration. Via diameter, Cu filling ratio, and Cu density were identified as important parameters in controlling the thermal stress distribution inside and around the TSVs.

In the second part, the fracture behavior of the 3D interconnects was investigated. Three probable failure modes were proposed and analyzed, including silicon z-cracking, r-cracking, and interface debonding between Cu TSV and silicon. The corresponding energy release rate and critical crack stress were deduced and compared to the fracture toughness of silicon and adhesion of TSV/silicon interface. Design guidelines of 3D interconnects with TSVs to improve thermal mechanical reliability were presented.

Chapter 6: Summary and Future Work

6.1 Summary

In this dissertation, the reliability issues caused by chip-package interaction were investigated for flip-chip packages. Experimental studies combined with finite element simulation were employed to research the thermal mechanical reliability of flip-chip packages. High-resolution moiré interferometry was used to measure the packaging induced deformation and stress in the package. Large thermal strain was observed in the solder/underfill layer, especially at the die corner. This strain concentration could lead to delamination between underfill and solder resist or silicon passivation. Selection of proper underfill materials becomes critical, especially when Pb-free solder and ultra low-k dielectrics were introduced into the flip-chip packages. A strategy study of underfill selection was conducted to find the proper underfills to reduce the risks of interfacial delamination in underfill and low-k interconnect structures under CPI while retaining reasonable solder fatigue life time.

The impacts of CPI on the mechanical reliability of Cu/low-k interconnects were investigated in chapter four. The discussion was first focused on the effects of dielectric and packaging materials including different low-k dielectrics and Pb-based and Pb-free solders. Packaging-induced crack driving forces for porous low-k layer delamination were deduced and compared with those for dense low-k dielectrics. Methods to improve the mechanical reliability of Cu/low-k interconnect under CPI were presented. The discussion is then extended to the scaling effect where the reduction of the interconnect dimension is accompanied by the use of more metal levels and the implementation of ultralow-k porous materials. Finally, some recent studies on CPI-induced crack

propagation in the low-k interconnect and the use of crack-stop structures to improve the chip reliability were discussed.

In chapter five, an emerging technology of 3D integration with through silicon vias (TSV) as the latest solution to improve the device density without down-scaling and its thermomechanical reliability were studied. The process-induced thermal stresses around TSVs in 3-D interconnect structures raise serious reliability issues such as device performance degradation and silicon cracking. Finite element analysis combined with bending beam experiments were employed to investigate the thermo-mechanical reliability problems. Firstly, process-induced residual stresses in TSV structures were calculated. Approaches to reduce the residual stress by optimizing the TSV geometry and configuration were presented. Via diameter, Cu fill ratio, and Cu density were identified as the most important parameters in controlling the thermal stress distribution inside and around the TSVs. The stress analysis was followed by a fracture study of 3D interconnects. Three probable failure modes were proposed and analyzed, including silicon z-cracking, r-cracking, and interface debonding between Cu TSV and silicon. The corresponding energy release rate and critical crack stress were deduced and compared to the fracture toughness of silicon and adhesion of TSV/silicon interface. Design guidelines of 3D interconnects with TSVs to improve thermal mechanical reliability were presented.

6.2 Future work

Chip-package interaction (CPI) is becoming a critical reliability issue for flip-chip packages with Cu/low-k chips and organic substrate. The thermo-mechanical reliability regarding underfill, Cu/low-k interconnects and solder bumps has attracted a lot of attentions. In this dissertation, virtual underfills were used to study the effect of Tg, E and

CTE on the solder fatigue life time, underfill delamination and low-k delamination, individually. A combined effect of all these factors is of great interest too. With new underfill materials being developed, it will be interesting to compare the reliability performance between these real underfill materials in addition to the virtual underfills.

In this dissertation, the introduction of Pb-free solder was found to have huge impacts on the reliability of Cu/low-k interconnects due to the higher stresses generated in the package compared to high Pb and eutectic solders. Recently a new bump structure called Cu pillar was adopted by Intel Corp. to enhance the electromigration performance of solder joints. Nevertheless, Cu pillar structure is mechanically stiffer than even Pb-free solders and thus more stresses can be transferred into the Cu/low-k interconnects during assembly. The impact of CPI on low-k reliability for flip-chip packages with Cu pillar bumps will be a big concern and an interesting topic to study.

3D Integration as an emerging solution can provide better electrical performance and heterogeneous integration of different subsystems. Thermo-mechanical reliability issues of 3D interconnect with Cu TSVs have raised many concerns. Three failure modes were proposed and analyzed in this dissertation. Further investigation on these failure modes is quite useful in order to optimize the structural design, especially for the interfacial delamination between Cu TSV and Si which turns out to be the most dominant failure mode now for the industry.

Appendix A: Sub-modeling Technique

The following introduction for sub-modeling technique is copied from ANSYS manual with minor changes

In finite element analysis, the finite element mesh is sometimes too coarse to produce satisfactory results in a specific region of interest, such as a stress concentration region in a stress analysis. To obtain more accurate results in such a region, you have two options: (a) reanalyze the entire model with greater mesh refinement, or (b) generate an independent, more finely meshed model of only the region of interest and analyze it. Obviously, option (a) can be time-consuming and costly (depending on the size of the overall model). Option (b) is the sub-modeling.

Submodeling is also known as the cut-boundary displacement method or the specified boundary displacement method. The cut boundary is the boundary of the submodel which represents a cut through the coarse model. Displacements calculated on the cut boundary of the coarse model are specified as boundary conditions for the submodel.

Submodeling is based on St. Venant's principle, which states that if an actual distribution of forces is replaced by a statically equivalent system, the distribution of stress and strain is altered only near the regions of load application. The principle implies that stress concentration effects are localized around the concentration; therefore, if the boundaries of the submodel are far enough away from the stress concentration, reasonably accurate results can be calculated in the submodel.

The ANSYS program does not restrict submodeling to structural (stress) analyses only. Submodeling can be used effectively in other disciplines as well. For example, in a

magnetic field analysis, you can use submodeling to calculate more accurate magnetic forces in a region of interest.

Aside from the obvious benefit of giving you more accurate results in a region of your model, the submodeling technique has other advantages:

- It reduces, or even eliminates, the need for complicated transition regions in solid finite element models.
- It enables you to experiment with different designs for the region of interest (different fillet radii, for example).
- It helps you in demonstrating the adequacy of mesh refinements.

Some restrictions for the use of submodeling are:

- It is valid only for solid elements and shell elements.
- The principle behind submodeling assumes that the cut boundaries are far enough away from the stress concentration region. You must verify that this assumption is adequately satisfied.

The process for using submodeling is as follows:

1. Create and analyze the coarse model.
2. Create the submodel.
3. Perform cut boundary interpolation.
4. Analyze the submodel.

5. Verify that the distance between the cut boundaries and the stress concentration is adequate.

1. Create and Analyze the Coarse Model

The first step is to model the entire structure and analyze it. The initial model is referred to as the coarse model. This does not mean that the mesh refinement has to be coarse, only that it is relatively coarse compared to the submodel. The analysis type may be static (steady-state) or transient and follows the same procedure as described in the individual analysis guides. Some additional points to keep in mind are listed below.

Jobname - You should use different jobnames for the coarse model and the submodel. This way, you can keep files from being overwritten. Also, you can easily refer to files from the coarse model during cut boundary interpolation.

Element Types -- Only solid and shell elements support the submodeling technique. Your analysis may include other element types (such as beams added as stiffeners), but the cut boundary should only pass through the solids or shells.

A special submodeling technique called *shell-to-solid* submodeling allows you to build your coarse model with shell elements and your submodel with 3-D solid elements. This technique is discussed in Shell-to-Solid Submodels.

Modeling -- In many cases, the coarse model need not include local details such as fillet radii, as shown in the following figure. However, the finite element mesh must be fine enough to produce a reasonably accurate degree of freedom solution. This is important because the results of the submodel are almost entirely based on interpolated degree of freedom results at the cut boundary.

Files - Both the results file (`Jobname.RST`, `Jobname.RMG`, etc.) and the database file (`Jobname.DB`, containing the model geometry) are required from the coarse-model analysis. Be sure to save the database before going on to create the submodel.

2. Create the Submodel

The submodel is completely independent of the coarse model. Therefore, the first step after the initial analysis is to clear the database at the Begin level. (Another way is to leave and re-enter the ANSYS program.) Also, be sure to use a different jobname for the submodel so that the coarse-model files are not overwritten.

Then enter PREP7 and build the submodel. Some points to remember are:

- Use the same element type (solid or shell) that was used in the coarse model. Also, specify the same element real constants (such as shell thickness) and material properties. (Another type of submodeling - shell-to-solid submodeling - allows you to switch from shell elements in the coarse model to 3-D solid elements in the submodel

- The location of the submodel (with respect to the global origin) must be the same as the corresponding portion of the coarse model.

  Specify appropriate node rotations. Node rotation angles on cut boundary nodes should *not* be changed after they have been written to the node file in interpolation step 1 (see Perform Cut-Boundary Interpolation).

Be aware that node rotation angles might be changed by application of nodal constraints [**DSYM**], by transfer of line constraints [**SFL**], or by transfer of area constraints [**SFA**], as well as by more obvious methods [**NROTAT** and **NMODIF**]. The presence or absence of node rotation angles in the coarse model has no effect upon the submodel. Loads and boundary conditions for the submodel will be covered in the next two steps.

3. Perform Cut-Boundary Interpolation

This is the key step in submodeling. You identify the nodes along the cut boundaries, and the ANSYS program calculates the DOF values (displacements, potentials, etc.) at those nodes by interpolating results from the full (coarse) model. For each node of the submodel along the cut boundary, the ANSYS program uses the appropriate element from the coarse mesh to determine the DOF values. These values are then interpolated onto the cut boundary nodes using the element shape functions.

The following tasks are involved in performing the cut boundary interpolation:

1. Identify and write the cut-boundary nodes of the submodel to a file (`Jobname.NODE` by default). You can do this in PREP7 by selecting nodes along the cut boundaries and then using one of NWRITE to write the nodes to a file.
2. Restore the full set of nodes, write the database to `Jobname.DB`, and leave PREP7. You must write the database to `Jobname.DB` because you need to continue with the submodel later.

3. To do the cut boundary interpolation (and the temperature interpolation), the database must contain the geometry for the coarse model. Therefore, you must resume the database using one of the methods shown below, making sure to identify the name of the coarse-model database file.
4. Enter POST1, which is the general postprocessor. Interpolation can only be performed in POST1.
5. Point to the coarse results file (**FILE** or menu path **Main Menu> General Postproc> Data & File Opts**).
6. Read in the desired set of data from the results file (**SET** or menu path **Main Menu>** General Postproc> Read Results> option).
7. Initiate cut-boundary interpolation by CBDOF command.
8. By default, the **CBDOF** command assumes that the cut boundary nodes are on file `Jobname.NODE`. The ANSYS program will then calculate the cut boundary DOF values and write them in the form of **D** commands to the file `Jobname.CBDO`.
9. All interpolation work is now done, so leave POST1 [**FINISH**] and restore the submodel database (**RESUME** or menu path **Utility Menu> File> Resume from**). (Be sure to use the submodel database jobname.)

4. Analyze the Submodel

In this step, you define the analysis type and analysis options, apply the interpolated DOF values (and temperatures), define other loads and boundary conditions, specify load step options, and obtain the submodel solution.

The first step is to enter SOLUTION (**/SOLU** or menu path **Main Menu> Solution**).

Then define the appropriate analysis type (usually static) and analysis options.

To apply the cut boundary DOF constraints, simply read in the file of **D** commands (created by **CBDOF**) using **/INPUT**,,CBDO.

It is important that you duplicate on the submodel any other loads and boundary conditions that existed on the coarse model. Examples are symmetry boundary conditions, surface loads, inertia forces (such as gravity), concentrated force loads, etc. Then specify load step options (such as output controls) and initiate solution calculations using SOLVE command.

Appendix B: Element Birth and Death Technique

The following introduction for sub-modeling technique is copied from ANSYS manual with minor changes

If material is added to or removed from a system, certain elements in your model may become "existent" or "nonexistent." In such cases, you can employ element birth and death options to deactivate or reactivate selected elements, respectively. The element birth and death feature is useful for analyzing excavation (as in mining and tunneling), staged construction (as in shored bridge erection), sequential assembly (as in fabrication of layered computer chips), and many other applications in which you can easily identify activated or deactivated elements by their known locations.

To achieve the "element death" effect, the ANSYS program does not actually remove "killed" elements. Instead, it deactivates them by multiplying their stiffness (or conductivity, or other analogous quantity) by a severe reduction factor (ESTIF). This factor is set to 1.0E-6 by default, but can be given other values. (For more information, see Apply Loads and Obtain the Solution.)

Element loads associated with deactivated elements are zeroed out of the load vector, however, they still appear in element-load lists. Similarly, mass, damping, specific heat, and other such effects are set to zero for deactivated elements. The mass and energy of deactivated elements are not included in the summations over the model. An element's strain is also set to zero as soon as that element is killed.

In like manner, when elements are "born," they are not actually added to the model; they are simply reactivated. You must create all elements, including those to be born in later stages of your analysis, while in PREP7. You cannot create new elements in

SOLUTION. To "add" an element, you first deactivate it, then reactivate it at the proper load step.

When an element is reactivated, its stiffness, mass, element loads, etc. return to their full original values. Elements are reactivated with no record of strain history (or heat storage, etc.); however, initial strain defined as a real constant (for elements such as LINK1) will not be affected by birth and death operations.

Unless large-deformation effects are activated (NLGEOM,ON), some element types will be reactivated in their originally specified geometric configuration. (Large-deformation effects should be included to obtain meaningful results.)

Thermal strains are computed for newly-activated elements based on the current load step temperature and the reference temperature. Thus, newborn elements with thermal loads may not be stress-free as intended. The material property REFT can be used instead of the global TREF to specify material-dependent reference temperatures, allowing you to specify the activation temperature as a stress-free temperature.

Employing Birth and Death

You can apply element birth and death behavior to most static and nonlinear transient analyses using the same basic procedures described in the various analysis guides. Modify your basic analysis procedure as follows to incorporate the element birth and death feature:

1. BUILD THE MODEL

While in /PREP7, create all elements - even those that will not be activated until later load steps. You cannot create new elements outside of /PREP7.

2. APPLY LOADS AND OBTAIN THE SOLUTION

For all analyses employing element birth and death, perform the following actions in the solution (SOLU) phase:

2.1. Define the First Load Step

In the first load step, you must choose the analysis type and all appropriate analysis options via the ANTYPE command.

For a structural analysis, activate large-deflection effects via the NLGEOM,ON command. For all birth and death applications, set the Newton-Raphson option to full explicitly in the first load step via the NROPT command. (The ANSYS program cannot predict the presence of an EKILL command in a subsequent load step.) Deactivate (EKILL) all of the initially inactive elements that you intend to add (reactivate) in later load steps.

Elements are deactivated (or activated) in the first substep of the load step, and maintain that status through the rest of the load step. The default reduction factor used as a stiffness multiplier might not suffice for some problems; sometimes, you may need to use a more severe reduction factor. To provide a new value for the reduction factor, issue the ESTIF command.

Nodes not connected to any active elements may "float," or pick up stray degree-of-freedom (DOF) responses. You may want to constrain inactive DOFs (D, CP, etc.) in some cases to reduce the number of equations to be solved and to avoid ill-conditioning. Constraining inactive DOFs can become more important for cases in which you want to reactivate elements with a specific shape (or temperature, etc.). If so, remove the artificial constraints when you reactivate elements, and remove nodal loads from inactive DOFs (that is, at nodes not connected to any active elements). Similarly, you must specifically add nodal loads (if any) to reactivated DOFs.

2.1.1. Sample Input for First Load Step

Part of your input listing could look like this for your first load step:

```
! First load step
TIME,...              ! Sets TIME value (optional for static analyses)
NLGEOM,ON             ! Turns large-deflection effects on
NROPT,FULL            ! You must explicitly set the Newton-Raphson option
ESTIF,...             ! Sets non-default reduction factor (optional)
ESEL,...              ! Selects elements to be deactivated in this load step
EKILL,...             ! Deactivates selected elements
ESEL,S,LIVE           ! Selects all active elements
NSLE,S                ! Selects all active nodes
NSEL,INVE             ! Selects all inactive nodes (those not attached to any
                      ! active elements)
D,ALL,ALL,0           ! Constrains all inactive DOFs (optional)
```

```
NSEL,ALL              ! Selects ALL nodes
ESEL,ALL              ! Selects ALL elements
D,...                 ! Adds constraints as appropriate
F,...                 ! Adds nodal loads to active DOFs as appropriate
SF,...                ! Adds element loads as appropriate
BF,...                ! Adds body loads as appropriate
SAVE
SOLVE
```

2.2. Define Subsequent Load Steps

In the remaining load steps, you can deactivate and reactivate elements as desired. As before, be sure to apply and delete constraints and nodal loads as appropriate.

To deactivate and reactivate elements, issue the EKILL and EALIVE commands, respectively.

2.2.1. Sample Input for Subsequent Load Steps

The following simplified input listing demonstrates how you might deactivate and reactivate elements:

```
! Second (or subsequent) load step:
TIME,...
ESEL,...
EKILL,...                  ! Deactivates selected elements
ESEL,...
```

```
EALIVE,...                  ! Reactivates selected elements
...
FDELE,...                   ! Deletes nodal loads at inactive DOFs
D,...                       ! Constrains inactive DOFs
...
F,...                       ! Adds nodal loads as appropriate to active DOFs
DDELE,...                   ! Deletes constraints from reactivated DOFs
SAVE
SOLVE
```

3. REVIEW THE RESULTS

Typically, you will follow standard procedures when postprocessing an analysis containing deactivated or reactivated elements.

Be aware that "killed" elements are still present in your model, even though they make an insignificant contribution to the stiffness (conductivity, etc.) matrix; therefore, they are included in element displays, output listings, etc. For example, deactivated elements are included in nodal results averaging (via the PLNSOL command) and will "smear" the results. Ignore the entire element printout for deactivated elements because many items computed make little physical sense.

To remove deactivated elements for element displays and other postprocessing operations, issue the ESEL command.

4. USE ANSYS RESULTS TO CONTROL BIRTH AND DEATH

At times, you will not explicitly know the location of elements that you need to deactivate or reactivate. For example, if you want to "kill" melted elements in a thermal analysis (that is, to model the removal of melted material), you will not know the location of those elements beforehand; you will need to identify them on the basis of their ANSYS-calculated temperatures. When the decision to deactivate or reactivate an element depends on the value of an ANSYS result item (such as temperature, stress, strain, etc.), you can use commands to identify and select the critical elements.

To identify the critical elements, issue the ETABLE command. To select the critical elements, issue the ESEL command.

You could then deactivate or reactivate the selected elements. To deactivate the selected elements, issue the EKILL,ALL command. To reactivate the selected elements, issue the EALIVE,ALL command.

4.1. Sample Input for Deactivating Elements

The following simplified input listing demonstrates how you might deactivate elements that rupture when their total strain has exceeded some critical value:

```
/SOLU                          ! Enter SOLUTION
RESCONTROL,DEFINE,NONE   ! Use single-frame restart
..                             ! Typical solution procedure
SOLVE
FINISH
!
```

```
/POST1                          ! Enter POST1
SET,...
ETABLE,STRAIN,EPTO,EQV    ! Store total equivalent strain in ETABLE
ESEL,S,ETAB,STRAIN,0.20 ! Select all elements with total equivalent strain
                          !    greater than or equal to 0.20
FINISH
!
/SOLU                           ! Re-enter SOLUTION
ANTYPE,,REST
EKILL,ALL                       ! Deactivate selected (overstrained) elements
ESEL,ALL                        ! Restore full element set
...                             ! Continue with solution
```

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